1. INTRODUCTION

1.1 General Description

The NCR 53C90 Enhanced SCSI Processor (ESP) is a high performance CMOS device which implements the ANSI X3.131-1986 SCSI Standard. The 53C90 operates in both the initiator and target roles and can therefore be used in host adapter and control unit applications.

The 53C90 performs such functions as bus arbitration, selection of a target or reselection of an initiator. It handles message, command, status and data transfer between the SCSI bus and its 16 byte internal FIFO or a buffer memory.

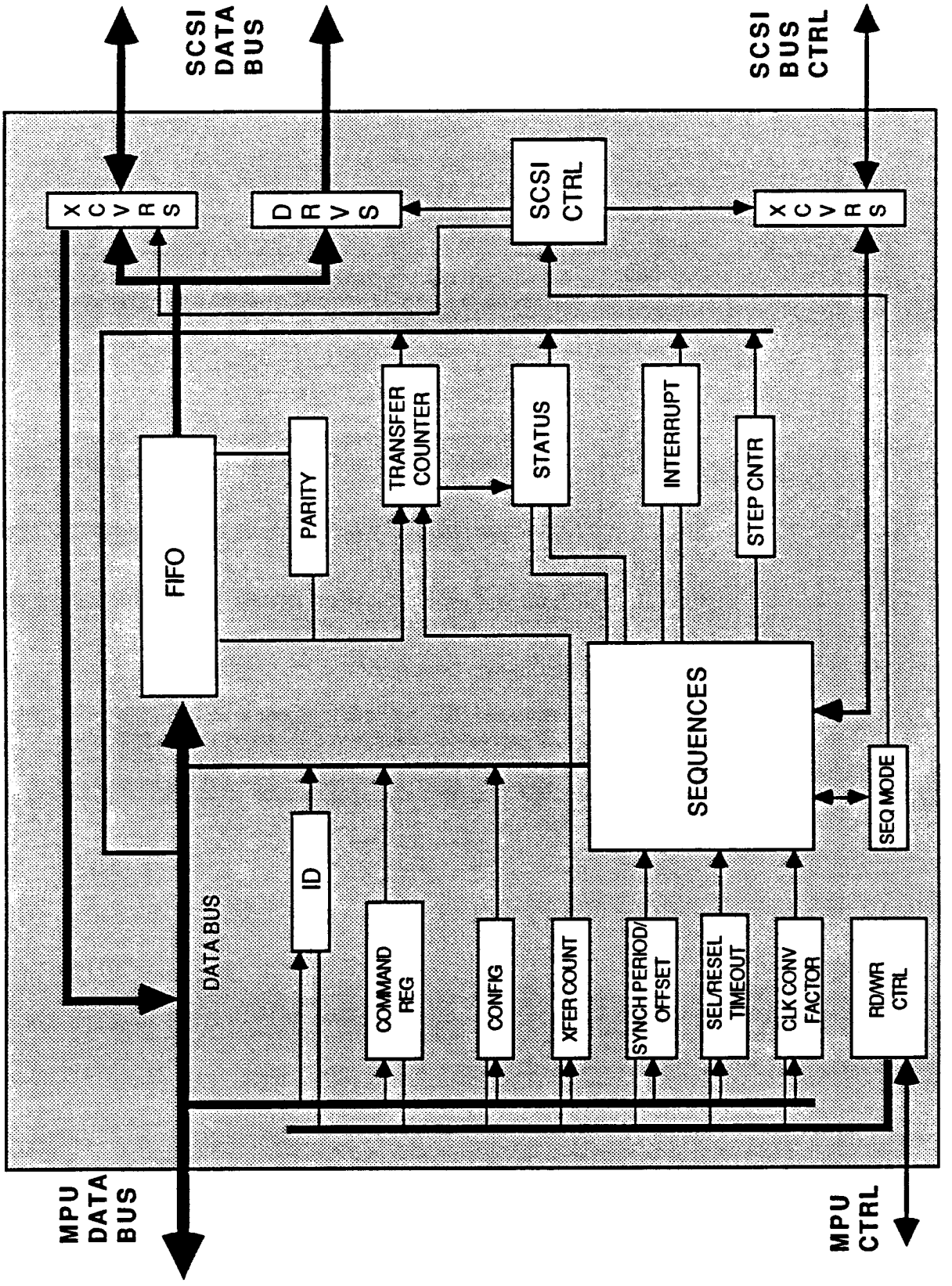
With its high level of integration, the ESP replaces SCSI interface circuitry, which typically consists of discrete devices, external drivers, and/or lower performance SCSI controllers.

The ESP maximizes protocol efficiency by utilizing a command pipeline, composed of a dual-ranked command register and transfer counter, and combination commands to minimize host intervention. The 53C90 also maximizes Transfer Rates by sustaining Asynchronous data rates over 3.0 MBytes/sec and Synchronous data rates of 5.0 MBytes/sec. With its on-chip 48 mA single-ended drivers and receivers, the ESP can be directly connected to the SCSI bus, hence minimizing board space requirement. The highly integrated structure utilized by the ESP provides several benefits to its users.

1.2 Enhanced SCSI Processor (ESP) Features Summary

- Support of ANSI X3.131-1986 SCSI standard
- Buffer Controller interface for I/O and fast DMA
- On-chip 48 mA single-ended drivers and receivers
- Control logic for differential transceivers
- Parity generation with optional checking
- Initiator and target roles supported
- Asynchronous data transfers over 3.0Mbytes per second
- Synchronous data transfers to 5.0Mbytes per second
  - Programmable synchronous transfer period
  - Programmable synchronous transfer offsets up to 15
- Sixteen-byte data FIFO between the DMA and SCSI channels
- Pipelined command structure
- Common SCSI sequences without microprocessor intervention
  - Selection sequence, from arbitration through command
  - Reselection sequence, from arbitration through message
  - Bus-initiated selection through received command
  - Bus-initiated reselection through received message
  - Command complete sequences
  - Terminate and disconnect sequences
- Interrupts microprocessor only when service is required
  - Disconnect or bus reset
  - Selection/reselection sequence complete
  - Target mode command complete or ATN detected
  - Initiator mode command complete or phase change detected
  - Waits until the phase is stable and REQ is asserted
- Clock rate up to 25 MHz
- Interfaces to eight-bit microprocessor data bus with minimal support logic
- CMOS low power requirements
- 68 pin PLCC and 80 pin QFP packages

1.3 Block Diagram



NCR 53C90 BLOCK DIAGRAM

2. ESP PIN DESCRIPTION

The ESP pins are described below. The pin type is indicated by "I" for input, "O" for output and "B" for bidirectional.

2.1 DMA Interface Pins

DMA Interface			
Pin #	**Type**	**Signal**	**Description**
4-1, 68-65	B	DB7-DB0	Active-high data bus connected to the DMA Controller, CPU and buffer memory. Each pad contains a pullup to Vdd (12.5K Ω minimum).
60-57	I	A3-A0	Active-high address bus which specifies one of the ESP's internal registers for reading or writing.
56	I	CS/	Active-low chip select signal which enables access to the ESP's internal registers. CS/ and DACK/ must never be active at the same time.
55	I	RD/	Active-low read signal which enables ESP data onto DB7-DB0. CS/ or DACK/ must also be active.
54	I	WR/	Active-low write signal which strobes DB7-DB0 data into the ESP. CS/ or DACK/ must also be active.
53	O	DREQ	Active-high DMA request to the DMA Controller.
52	I	DACK/	Active-low DMA acknowledge signal from the DMA Controller. CS/ and DACK/ must never be active at the same time.
61	O	INT/	Active-low, open drain interrupt signal to the microprocessor.

2.2 Miscellaneous Pins

Miscellaneous Pins			
Pin #	**Type**	**Signal**	**Description**
50	O	IGS	Active-high initiator group select signal. This pin is high whenever the ESP is in initiator mode. It is used in differential mode to enable the initiator signals (ACKO/, ATNO/). When low the ESP should be receiving these signals.
49	O	TGS	Active-high target group select signal. This pin is high whenever the ESP is in target mode. It is used in differential mode to enable the target signals (REQO/, MSGO/, CDO/, IOO/). When low the ESP should be receiving these signals.
5	I	DIFFM	Differential mode enable. When this pin is grounded the ESP operates in single-ended mode, with separate SCSI data input and output buses. When this pin is high the ESP operates in differential mode, with bidirectional SCSI data on the SDI pins and active high differential transceiver enables on the SDO pins.
63	I	RESET	Active-high chip reset. When this pin is high the ESP registers and sequencers are initialized. This pin must not be connected to the RESETO pin.
62	O	RESETO	Active-high reset output. This pin is asserted whenever the RESET input pin is active. It is also asserted when a SCSI reset interrupt timeout occurs.
51	I	CLK	Square wave clock which generates internal chip timing. The maximum frequency is 25 MHz. For synchronous transfers, the minimum is 13 MHz. A minimum of 10MHz is required for asynchronous transfers.
15, 48		VDD	+5V power input (2 pins)
16, 21 27, 32 38, 64		VSS	Ground reference (6 pins)

2.3 SCSI Bus Interface Pins

SCSI Bus Interface			
Pin #	Type	Signal	Description
25-22 20-17	O	SDO7/-SDO0/	48 mA, open drain SCSI data/parity bus. In single-ended mode (DIFFM=0), these pins output active-low data signals to the SCSI bus. In differential mode (DIFFM=1), these pins are used to control the direction of external differential transceivers. When a pin is high, the direction is out to the SCSI bus.
26	O	SDOP/	
13-6 14	B	SDI7/-SDI0/ SDIP/	Schmitt trigger, active-low SCSI data/parity bus. In single-ended mode (DIFFM-0), these pins are used strictly for input from the SCSI bus. In differential mode (DIFFM=1), these pins carry bidirectional data/parity to and from the external SCSI bus transceivers.
28	O	SELO/	48 mA, open drain SCSI select signal. In single-ended mode, this pin is active low. In differential mode, this pin is active high. The pin is asserted by the chip when it attempts to select or reselect a SCSI device.
29	O	BSYO/	48 mA, open drain SCSI busy signal. In single-ended mode, this pin is active low. In differential mode, this pin is active high.
36	O	ATNO/	48 mA, open drain, active-low SCSI attention signal. This pin is only asserted when the ESP is in initiator mode.
31	O	ACKO/	48 mA, open drain, active-low SCSI acknowledge signal. This pin is only asserted when the ESP is in the initiator mode.
30	O	REQO/	48 mA, open drain, active-low SCSI request signal. This pin is only asserted when the ESP is in target mode.
33-35	O	MSGO/, CDO/, IOO/	48 mA, open drain, active-low SCSI phase signals. These pins are only asserted when the ESP is in target mode.
37	O	RSTO/	48 mA, open drain SCSI reset signal. In single-ended mode, this pin is active low. In differential mode, this pin is active high.
39	I	SELI/	Schmitt trigger, active-low SCSI select signal.
40	I	BSYI/	Schmitt trigger, active-low SCSI busy signal.
41	I	REQI/	Schmitt trigger, active-low SCSI request signal.
42	I	ACKI/	Schmitt trigger, active-low SCSI acknowledge signal.
43	I	MSGI/	Schmitt trigger, active-low SCSI message signal.
44	I	CDI/	Schmitt trigger, active-low SCSI control/data signal.
45	I	IOI/	Schmitt trigger, active-low SCSI input/output signal.
46	I	ATNI/	Schmitt trigger, active-low SCSI attention signal.
47	I	RSTI/	Schmitt trigger, active-low SCSI reset signal.

2.4 Differential Mode Enable Pin

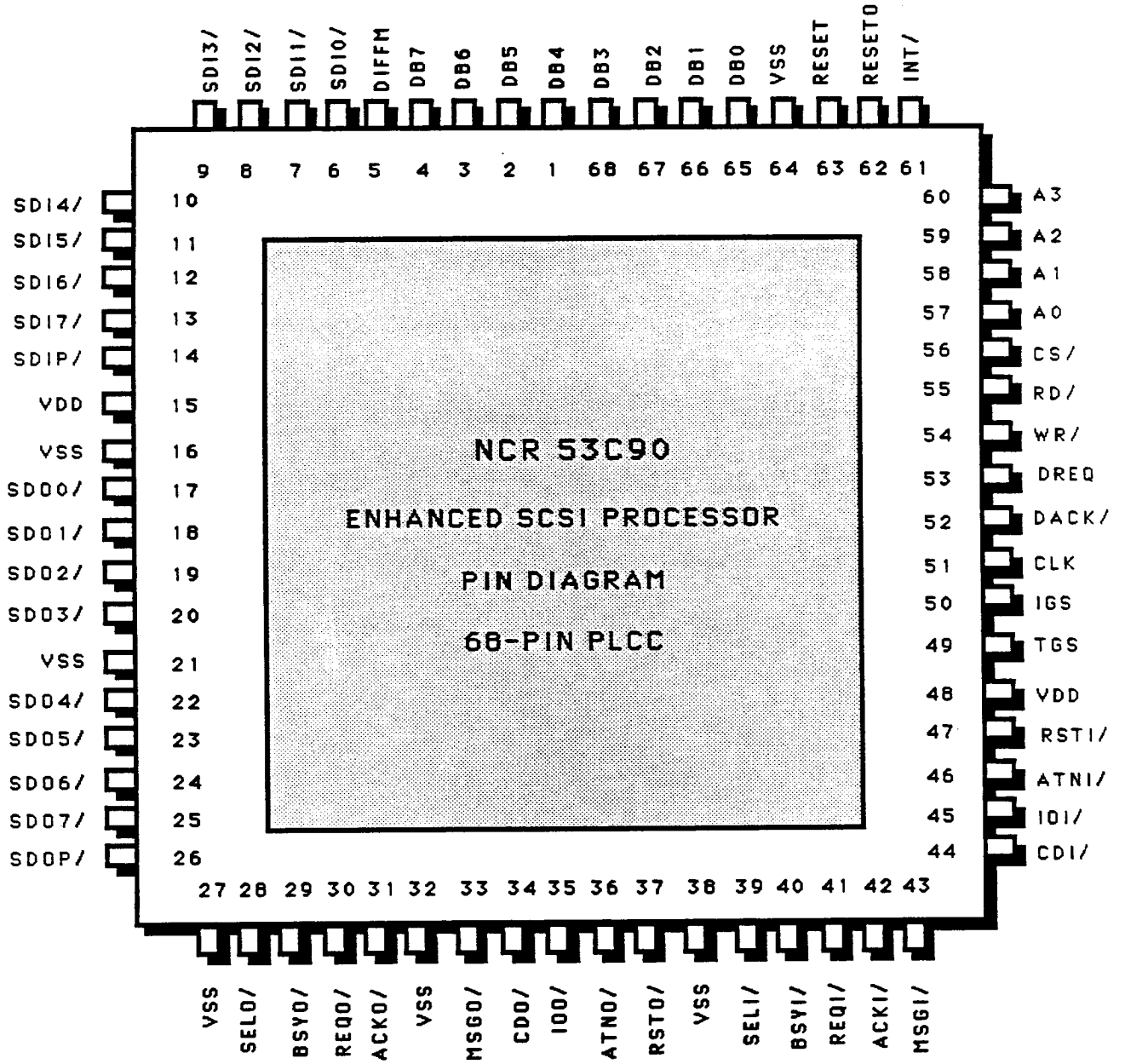
The differential mode enable pin alters the SCSI data paths in the ESP. When the pin is grounded, the ESP operates in single-ended mode with the SDI and SDO buses providing separate input data and output data, respectively. That is, the ESP drives data out on SDO7/-SDO0/ and receives data on SDI7/-SDI0/. The SCSI data and control pins are all negative true.

When the differential mode enable pin is high, the SDI bus becomes a bidirectional data bus and the SDO bus is used to control the external differential transceivers. The transceivers have positive true output enables and negative true input enables. They are configured as all driving or all receiving, except during arbitration when only the bus ID bit is driven and all other bits are received. In addition, the polarity of the RSTO/, SELO/, and BSYO/pins are set to positive true to enable external differential drivers for these signals.

Since the TGS and IGS output pins are true when the ESP is in target or initiator mode, respectively, they may be used to enable external differential drivers for the target and initiator groups of signals:

Target Signals	Initiator Signals
REQO/	ACKO/
MSGO/	ATNO/
CDO/	
IOO/	

2.5 ESP 68 Pin PLCC Pin Diagram



3. USER-ACCESSIBLE REGISTER AND COUNTERS

The ESP has a number of registers which are used to configure, command, monitor, and pass data to the chip. These registers are listed in the table below and more fully described in the paragraphs that follow.

#	Read	Write
0	Transfer counter lo (LSB)	Transfer count lo (LSB)
1	Transfer counter hi (MSB)	Transfer count hi (MSB)
2	FIFO	FIFO
3	Command	Command
4	Status	Select/reselect bus ID
5	Interrupt status	Select/reselect timeout
6	Sequence step	Sync period
7	FIFO flags	Sync offset
8	Configuration	Configuration
9	NCR Reserved	Clock conversion factor
A	NCR Reserved	Test

3.1 Transfer Counter - Address 0,1 (Read only)

This 16-bit counter is used by the DMA commands and by the the command sequence. It is loaded at the beginning of a DMA command (the contents of the Transfer Count Register is loaded into it) and when receiving a SCSI command (it is loaded with the decoded length of the command). The counter may be read to help determine the number of bytes remaining to be transferred if a sequence terminates early.

3.2 Transfer Count Register - Address 0,1 (Write only)

This 16-bit register is normally loaded prior to writing a command to the Command Register. The value in this register is transferred to the Transfer Counter at the beginning of a command which uses DMA. The Transfer Count need only be loaded once for successive DMA commands using the same count. Zero specifies maximum count (65536).

3.3 FIFO Register - Address 2 (Read/Write)

The FIFO is a 16-byte deep, first-in-first-out buffer between the SCSI bus and buffer memory. It is accessible by the microprocessor via this register.

3.4 Command Register - Address 3 (Read/Write)

The Command Register is an eight-bit read/write register used to give commands to the ESP. The register is double ranked, enabling the microprocessor to stack commands to the ESP. Once the bottom command has been completed and reported, the top command (if present) will fall to the bottom and execute. The value of the last executed (or executing) command will be contained in the bottom of the Command Register.

Bit 7 Enable DMA
When this bit is reset (0) and sending, the chip transmits data to the SCSI bus from the FIFO until it is empty. It does not modify the transfer counter.

When this bit is reset (0) and receiving, the chip receives a single byte into the FIFO. It does not modify the transfer counter.

When this bit is set (1) and sending, data will be transferred through the DMA channel into the FIFO. The counter is decremented as bytes are received by the DMA channel. Data will continue to be transmitted to the SCSI bus from the FIFO until it is empty and the transfer counter is zero.

When this bit is set (1) and receiving, the chip receives from the SCSI bus the number of bytes specified in the transfer counter into the FIFO, decrementing the transfer counter as bytes are received. Data will be transferred to the DMA channel from the FIFO until it is empty and the transfer counter is zero.

When this bit is receiving synchronous data in the Initiator mode, the transfer counter is decremented as bytes are removed by the DMA channel. The transfer completes when the transfer counter is zero.

Bit 6-0 Command Code
The ESP responds to 26 commands, by which the microprocessor can initiate data transfers, prepare the controller for selection, etc. Bits 6-4 specify the command mode:

Bit 6 Disconnected Mode

Bit 5 Target Mode

Bit 4 Initiator Mode

Bits 3-0 specify the command within the mode group.

3.4.1 Command Summary

The ESP's Command set is listed in the following table.

Bits 7 6 5 4 3 2 1 0	Command	Int
	MISC	
x 0 0 0 0 0 0 0 0	NOP	no
x 0 0 0 0 0 0 0 1	Flush FIFO	no
x 0 0 0 0 0 1 0	Reset Chip	no
x 0 0 0 0 0 1 1	Reset SCSI bus	no*
	DISCONNECTED	
x 1 0 0 0 0 0 0 0	Reselect sequence	yes
x 1 0 0 0 0 0 0 1	Select without ATN sequence	yes
x 1 0 0 0 0 1 0	Select with ATN sequence	yes
x 1 0 0 0 0 1 1	Select with ATN and stop sequence	yes
x 1 0 0 0 1 0 0	Enable selection/reselection	no
x 1 0 0 0 1 0 1	Disable selection/reselection	yes
	TARGET	
x 0 1 0 0 0 0 0	Send message	yes
x 0 1 0 0 0 0 1	Send status	yes
x 0 1 0 0 0 1 0	Send data	yes
x 0 1 0 0 0 1 1	Disconnect sequence	yes
x 0 1 0 0 1 0 0	Terminate sequence	yes
x 0 1 0 0 1 0 1	Target command complete sequence	yes
x 0 1 0 0 1 1 1	Disconnect	no
x 0 1 0 1 0 0 0	Receive message sequence	yes
x 0 1 0 1 0 0 1	Receive command	yes
x 0 1 0 1 0 1 0	Receive data	yes
x 0 1 0 1 0 1 1	Receive command sequence	yes
	INITIATOR	
x 0 0 1 0 0 0 0	Transfer information	yes
x 0 0 1 0 0 0 1	Initiator command complete sequence	yes
x 0 0 1 0 0 1 0	Message accepted	yes
x 0 0 1 1 0 0 0	Transfer pad	yes
x 0 0 1 1 0 1 0	Set ATN	no

*External connection of the RSTO/ pin to RSTI/ pin causes an interrupt if the SCSI reset interrupt is not disabled in the Configuration Register.

An illegal interrupt is generated if the ESP is not currently in the mode specified by bits 6-4, or if bits 3-0 specify an unsupported command.

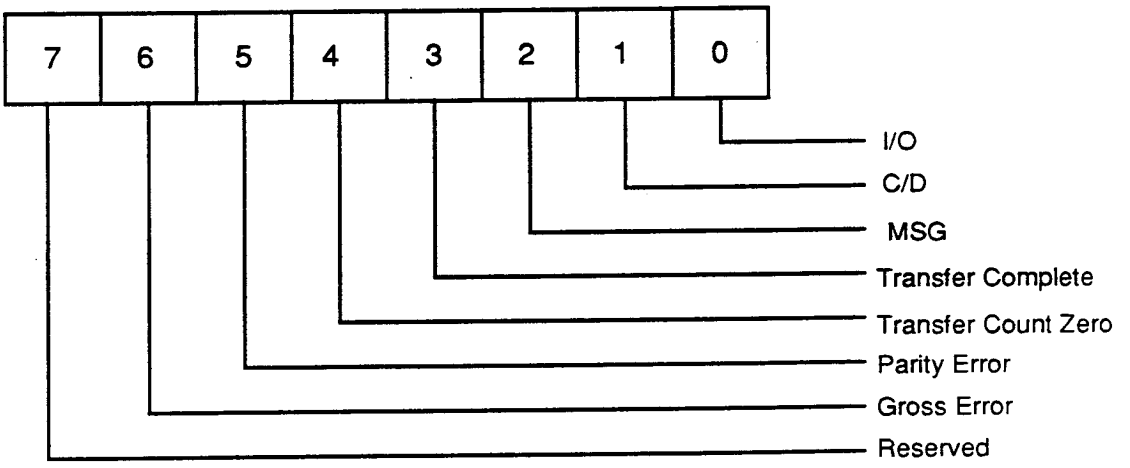
Certain conditions clear the Command Register, as summarized below:

- Chip reset
- SCSI bus reset or disconnect
- Completion of bus-initiated selection or reselection
- Completion of a select command
- Completion of a Reselect Command if ATN is asserted
- Select or reselect timeout
- Completion of a target disconnect or terminate command
- Bad parity received in the target mode
- Assertion of ATN in target mode
- Phase change during an initiator transfer
- Unexpected phase change during an initiator sequence
- Illegal command

Note the RESET chip and RESET SCSI Bus commands execute as soon as they are loaded into the top of the Command Register.

3.5 Status Register - Address 4 (Read only)

This eight-bit read-only register contains fields to indicate the status of the chip and to qualify the reason for an interrupt. Because several of these fields are reset when the Interrupt Register is read, the Status Register should always be read prior to the Interrupt Register. The fields within the Status Register are defined below.



Bit 7 Reserved

Bit 6 Gross Error
This status bit is set (1) when one of the following has occurred:

1. The top of the FIFO has been overwritten
2. The top of the Command Register has been overwritten
3. A DMA transfer occurs in the wrong direction
4. A phase change occurs in the middle of an initiator synchronous data transfer.

No interrupt is generated by the ESP when a gross error is detected. Bit 6 resets (0) if the Interrupt Register is read when the interrupt pin is active.

Bit 5 Parity Error
This bit is set to a one when parity is enabled in the Configuration Register and the ESP detects a parity error on a byte received from the SCSI bus. It is cleared if the Interrupt Register is read when the interrupt pin is active.

Bit 4 Transfer Count Zero
This bit is set (1) when the Transfer Counter decrements to zero. It resets when the Transfer Counter is loaded.

Bit 3 Transfer Complete
This status bit is set to a one during the target command sequence if the received command is in one of the non-reserved groups (0, 1, 5, 6 or 7). It is reset, if the Interrupt Register is read when the interrupt pin is active.

Bits 2-0 SCSI Phase
Bits 2 through 0 indicate the state of the SCSI MSG, C/D and I/O signals, respectively. These bits define the information phase being asserted by the target.

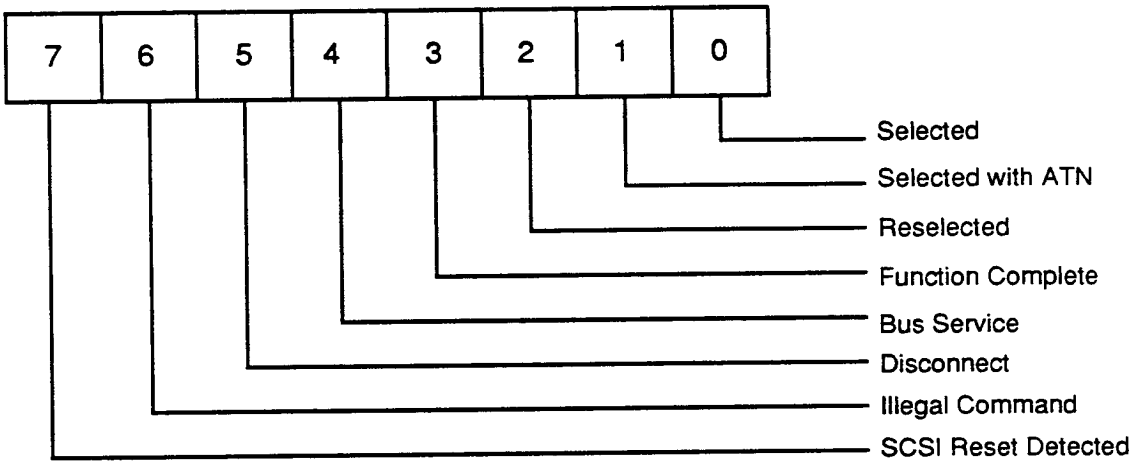
Bits 2 1 0	SCSI Bus Phase
0 0 0	Data out
0 0 1	Data in
0 1 0	Command
0 1 1	Status
1 0 0	Reserved for future standardization
1 0 1	Reserved for future standardization
1 1 0	Message out
1 1 1	Message in

3.6 Select/Reselect Bus ID Register - Address 4 (Write only)

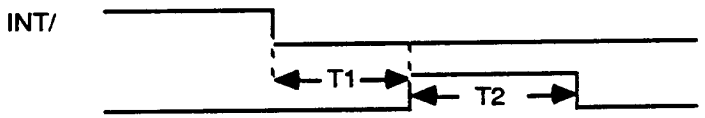
The Select/Reselect Bus ID Register is a three-bit write-only register which specifies the encoded destination bus ID for a Select or Reselect command. (least significant 3 bits)

3.7 Interrupt Status Register - Address 5 (Read only)

This eight-bit read-only register is used in conjunction with the Status Register and Sequence Counter to determine the cause of an interrupt.



Bit 7 SCSI Reset Detected
This bit is set if the SCSI reset interrupt disable bit is zero in the Configuration Register and the chip detects a reset on the SCSI bus. If the interrupt is not serviced in T1 ms, the chip will assert RESETO for T2 µs. (See below)



T1 = 2 (Clock Period) [(Clock Conversion Factor •3841)-1]

T2 = 2 (Clock Period) [(65)(Clock Conversion Factor)]

Example: Clock = 24MHz, CCF = 5

T1 = 1.60033ms
T2 = 27.0833µs

Bit 6 — Illegal Command
This bit is set when the ESP detects an unused code or illegal command.

Bit 5 — Disconnect
Ths bit is set when the ESP is in initiator mode and the target disconnects from the bus, or if a selection or reselection timeout occurs. In the target mode, this bit is set when the Terminate Sequence or Command Complete Sequence command disconnects the ESP from the SCSI bus.

Bit 4 — Bus Service
In target mode, this bit is set when the ATN signal is asserted, indicating the initiator is requesting service. In initiator mode, this bit will be set on command completion unless a message is received and ACK is still asserted.

Bit 3 — Function Complete
This bit is set to indicate that an interrupting-type disconnected or target state command has completed. In initiator mode, this bit will be set when a message has been received and ACK is being asserted.

Bit 2 — Reselected
This bit is set to indicate the chip has been reselected as an initiator.

Bit 1 — Selected with ATN
This bit is identical to the selected bit except it indicates that the initiator asserted ATN during selection.

Bit 0 — Selected
This bit is set to indicate the chip has been selected as as a target.

Reading the Interrupt Register while the interrupt pin is active, causes the interrupt pin, Interrupt Status Register, and Sequence Step Registers to be cleared. Always read the Status Register (and the Sequence Step Register) prior to reading the Interrupt Register. If the ESP is waiting for the interrupt to be cleared to report the status of its command, the interrupt pin will be reasserted.

3.8 Select/Reselect Timeout Register - Address 5 (Write only)

The Select/Reselect Timeout Register is an eight-bit write-only register which specifies the amount of time to wait for a response during selection or reselection. This register is typically loaded to specify a timeout period of 250 ms (93H at 24 MHz). To determine the value for other timeouts use the following equation:

8192*CCF*tcp = TU

T/TU = Register Value (convert to Hex)

Where: CCF = Clock Conversion Factor (See section 3.14)
tcp = Input Clock Period
TU = Time Unit
T = Desired Timeout

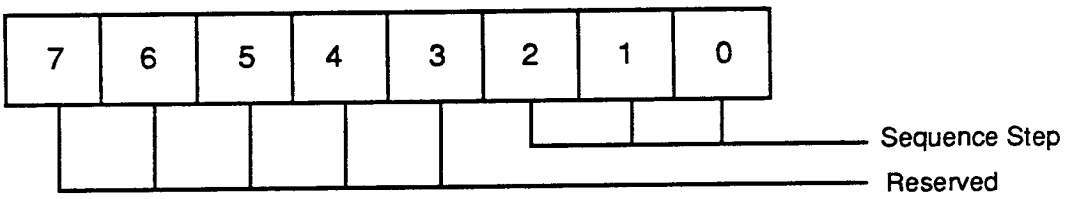
Note: Maximum timeout = 255TU

3.9 Sequence Step - Address 6 (Read only)

The Sequence Step Register is an eight-bit read-only register which indicates the current substep within certain ESP sequences when an interrupt occurs. The least significant three bits form an incrementing sequence to indicate which steps of a sequence were executed prior to the interrupt. The upper five bits are reserved. (Refer to Section 7.1)

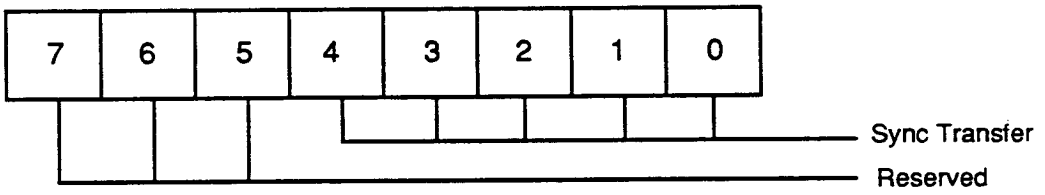
The sequences that utilize this register are:

Target	Initiator
Bus Initiated Selection with ATN	Bus Initiated Selection
Receive Command Sequence	Select with ATN
Command Complete Sequence	Select with ATN and Stop
Disconnect Sequence	Select without ATN
Terminate Sequence	



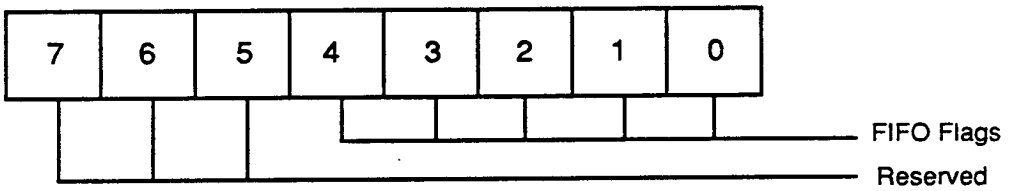
3.10 Synchronous Transfer Period Register - Address 6 (Write only)

The Synchronous Transfer Period Register is a five-bit write-only register which specifies the minimum time between leading edges of successive REQ or ACK pulses. The time unit is the input clock period. The minimum transfer period is five cycles and the maximum is 35 cycles. The default value is five cycles.



3.11 FIFO Flags Register - Address 7 (Read only)

This is a read-only register. The least significant five bits encode the sixteen FIFO full flags to indicate the number of bytes remaining in the FIFO. The remaining bits are reserved.

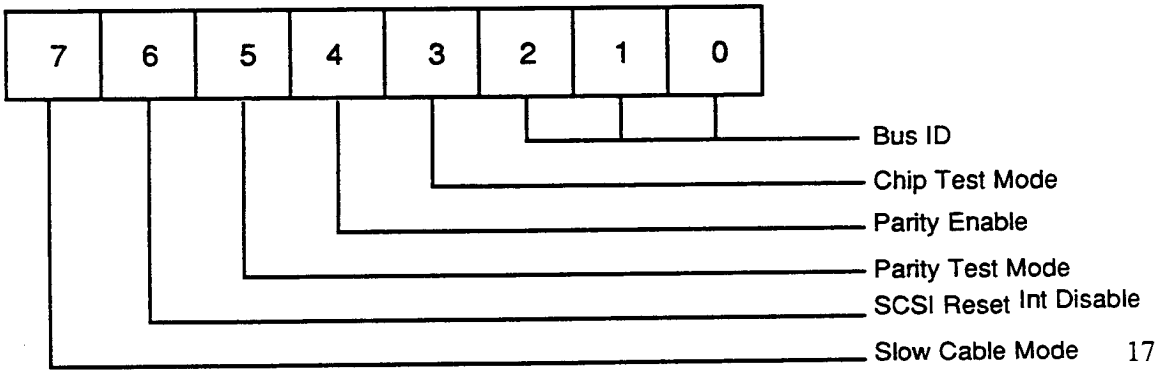


3.12 Synchronous Offset Register - Address 7 (Write only)

The Synchronous Offset Register is a four-bit write-only register (bits 3-0) which specifies the maximum REQ/ACK offset allowed during synchronous transfers. An offset of zero specifies an asynchronous operation.

3.13 Configuration Register - Address 8 (Read/Write)

This eight-bit read/write register is used to specify different operating options for the ESP. The bits are defined below.



Bit 7 Slow Cable Mode
When set, this bit increases the minimum data setup time from two cycles to three when transmitting to the SCSI bus. The minimum asynchronous and synchronous transmit periods are also increased to four and six cycles, respectively. This bit should be enabled if excessive capacitance on the SCSI cable causes SCSI timing violations.

Bit 6 SCSI Reset Interrupt Disable
This bit disables the reporting of a SCSI reset condition. If a SCSI reset occurs with this bit set, the ESP will disconnect from the SCSI bus and remain in the idle state without reporting an interrupt or timing out the response.

Bit 5 Parity Test Mode
This bit causes the parity output to the SCSI bus to be generated from Bit 7 of the transmitted byte, rather than from the parity generator. This facilitates system debug by allowing the MPU to force bad parity on any byte. This bit must not be enabled in normal operation.

Bit 4 Parity Enable
When set (1), this bit enables parity checking whenever data is read from SCSI bus except during arbitration and when receiving pad bytes.

Bit 3 Chip Test Mode
When set (1), this bit enables special test circuitry which is used during chip test (see Section 3.15). This mode must not be enabled in normal operation.

Bits 2-0 Bus ID
The bus ID is a three-bit field which specifies the encodedvalue of the SCSI Bus ID to which the ESP chip responds during a bus-initiated selection or reselection, and the bus ID to assert during arbitration and selection or reselection.

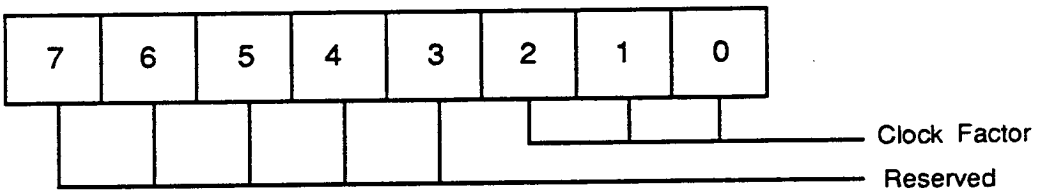
3.14 Clock Conversion Register - Address 9 (Write only)

The Clock Conversion Factor is a three-bit write-only register which is used for generating all timings in the ESP longer than 400 ns. The Clock Conversion Factor must never be loaded with the value 1.

Clock Conversion Factor = 200/tcp

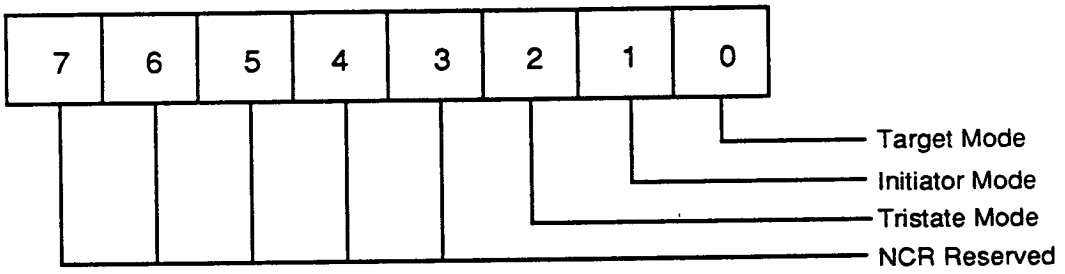
Where: tcp = input clock period (ns)

CLK Freq (MHz)	CLK Conv. Factor
10	2
10.01 to 15	3
15.01 to 20	4
20.01 to 25	5



3.15 Test Register - Address A (Write only)

This write only register utilizes the least significant three bits to place the chip in various modes for testing. To set these bits, first put the ESP into test mode by setting bit 3 of the Configuration Register. Next load the appropriate bit value into the Test Register. To clear the test mode, the ESP must be reset by either asserting the RESET input or issuing a RESET chip command. Caution must be exercised when using this register.



Bit 2 — Tri-State Test Mode
This mode allows the ESP to support board-level automatic testing. When this bit is set, all bidirectional and output pins are forced into a high impedance state, regardless of the chip inputs.

Bit 1 — Initiator Mode
This bit, when set, will put the ESP into the initiator mode.

Bit 0 — Target Mode
When this bit is set, the ESP is placed into the target mode.

4. SEQUENCER

The sequencer modules are briefly described below. These modules are used internally by the ESP and are not user accessable. However, they are used by commands/registers as described. Refer to the functional description section for more information. (See Section 6)

4.1 Bus Delay Module

The bus delay module detects whether the SCSI bus has been in the bus free state for more than a bus settle delay plus a bus free delay (1200 ns min).

The module also generates the timing for a bus settle delay (400 ns min), an arbitration delay (2200 ns min), a reset hold delay (25 µs min), a selection abort delay (200 µs), and the select/reselect timeout clock (1.7 ms). The module contains a twelve bit counter clocked by the conversion clock to generate the timing.

4.2 Phase Monitor Module

The phase monitor module monitors the SCSI bus to detect phase changes. If the ESP is an initiator and BSY and SEL are both released, a disconnect interrupt is generated and the sequencer is halted.

4.3 DMA Controller Interface

The DMA controller interface performs the actual transfers over the DMA channel. The module is coupled to the transfer counter and the FIFO.

4.4 SCSI Interface Modules

The SCSI interface modules perform the actual transfers over the SCSI bus. The mode of operation depends on whether the transfers are synchronous or asynchronous, single or multi-byte, target or initiator, and single ended or differential. The SCSI interface modules are coupled to the Transfer Counter, the FIFO, Synchronous Transfer Period Counter, and Synchronous Offset Counter. These modules are used internally by the ESP and are not accessible. However, these are used by the various commands/registers.

Odd parity is generated for the SCSI data out bus. If the number of asserted data bits is even, the parity bit is asserted. Parity is checked on the SCSI data-in bus if parity checking is enabled in the Configuration Register. During arbitration and when receiving pad bytes, parity is not checked.

4.5 Bus Initiated Selection/Reselection

The Bus Initiated Selection/Reselection sequence responds to selection by a SCSI initiator, incuding checking for and receiving an identify message and a command block. It also responds to reselection by a SCSI target, including checking for and receiving a message byte.

4.6 Command Sequence

The Command Sequence module decodes the length of an incoming command from information in the first byte, loads the transfer counter, and receives the appropriate number of bytes as described in the functional description. (See Section 6)

4.7 Disconnected State Commands

The Disconnected State Commands module arbitrates and selects a SCSI target with optional message and command transmission, or reselects a SCSI initiator with message byte transmission, as described in the functional description. (See Section 6.3.1)

4.8 Target Commands

The Target Commands module implements the target mode commands, as described in the functional description. (See Section 6.3.2)

4.9 Initiator Commands

The Initiator Commands module implements the initiator mode commands, as described in the functional description. (See Section 6.3.3)

5. MISCELLANEOUS BLOCKS

The following section describes various functional blocks that are utilized within the ESP. These modules/blocks are for information only and are not user accessable.

5.1 ID Module

The ID module determines whether there is an ID match by using the three-bit bus ID contained in the configuration register to pick a bit in the SCSI data-in bus. It also determines if the proper number of bits are set.

The ID module also checks the SCSI data bus for a set bit which is higher than the bus ID contained in the configuration register. If there is none, the ESP has won arbitration.

If the ESP is in the Arbitration Phase, the ID module generates the destination ID which is the OR of the arbitration ID and the decoded select/reselect bus ID. The parity bit is always asserted, which forces bad parity if the select/reselect ID is inadvertently set equal to the arbitration ID.

5.2 Read/Write Control

The Read/Write Control Module handles the I/O interface with the DMA Controller when the microprocessor wishes to access one of the user-accessible registers in the ESP.

5.3 Select/Reselect Timer

The Select/Reselect timer is an eight-bit timer which is clocked by the sequencer bus delay module. With a 24 MHz chip clock, the timer is clocked approximately once every 1.7 ms. The timer is compared with the Select/Reselect Timeout Register to determine whether a select/reselect timeout has occurred. (See Section 3.8)

5.4 Synchronous Offset Counter

The synchronous offset counter is a four-bit up/down counter used to control synchronous data transfers.

The offset counter also contains logic to detect whether the counter is zero or if it is equal to the contents of the synchronous offset register.

5.5 Command Decode

The command decode circuit decodes bits 7-5 of the first byte received in the command phase to determine the command group and thus the length of the incoming command. The byte is decoded from the top of the FIFO.

SCSI Command Block Description

Group	Bytes Stored	Description
0	6	Six-byte command
1	10	Ten-byte command
2	6	Reserved
3	6	Reserved
4	6	Reserved
5	12	Twelve-byte command
6	6	Vendor unique (six bytes)
7	10	Vendor unique (ten bytes)

5.6 Sequencer Mode Register

The Sequencer Mode Register stores information about the sequencer. The fields within the register are defined below.

Target
Indicates that the ESP is a target. This bit drives the TGS output pin which controls the target group of transceivers when operating with differential drivers.

Initiator
Indicates that the ESP is an initiator. This bit drives the IGS output pin which controls the initiator group of transceivers when operating with differential drivers.

Select/Reselect Enable
Indicates that the ESP has received an Enable Selection/Reselection command, enabling it to perform the bus-initiated selection and reselection sequences.

Select/Reselect DMA Enable
Indicates that the Enable Selection/Reselection command was issued with the DMA bit set. If this bit is set and the microprocessor issues a Select or Reselect command with DMA, an illegal command interrupt is generated.

6. FUNCTIONAL DESCRIPTION

The following section contains the functional descriptions for the ESP including Bus Initiated Sequences, Commands and Flow Charts.

6.1 Initialization

The ESP has three levels of reset. The hard reset (H), applied when the reset pin is high or when a Reset Chip command is executed, resets the entire chip. The soft reset (R), applied when HRST or SCSI bus reset is active, resets a subset of the functions reset by the hard reset. The disconnect reset (D), applied when the soft reset is active or a disconnect occurs, resets a subset of the functions reset by the soft reset.

Initialization for Different Levels of Reset

Reset	Description
H	Set clock conversion factor to 2
	Clear configuration register bits:
H	Chip test mode = 0
H	Parity enable = 0
H	Parity test mode = 0
H	SCSI reset interrupt disable = 0
H	Slow cable mode = 0
H	Initialize FIFO to empty
H	Set synchronous period to 5
H	Set synchronous offset to 0
H	Release SCSI RSTO signal*
H	Release interrupt pin
H	Clear interrupt register to 0
	Clear status register bits:
H	Transfer complete = 0
H	Parity error = 0
H	Gross error = 0
HR	Transfer count zero = 0
HR	Reset DMA interface
HR	Reset bus-initiated selection/reselection module
HR	Reset command sequence module
HR	Reset sequence step
	Clear sequencer mode bits:
HR	Enable sel/resel = 0
HRD	Target = 0
HRD	Initiator = 0
HRD	Initialize command register FIFO to empty
HRD	Release all SCSI signals*
HRD	Reset disconnect, initiator, and target command modules

*Note: RSTO/ is only released by a Hard (H) reset

When the RESET input signal is asserted, it is recognized immediately by the ESP, but the chip releases it internally in a synchronous manner, 0.5 to 1.5 cycles after RESET is released. RESET must be asserted for a minimum of two clock cycles.

The reset output pin, RESETO, is the OR of RESET and the SCSI reset interrupt timeout, described in section 6.2.3. RESETO is generally used to reset the microprocessor and other on-board circuitry.

The microprocessor should program the following registers as part of its start up procedure:

- Configuration Register
- Clock Conversion Factor

The microprocessor must initialize the following registers prior to their use, since they are not initialized by a chip reset:

- Bus ID (in the Configuration Register)
- Transfer Count low and high bytes
- Select/Reselect bus ID
- Select/Reselect timeout

6.2 Bus Initiated Sequences

BUS INITIATED SEQUENCES
Selection
Reselection
SCSI Bus Reset

Bus Initiated sequences occur during the disconnected state when the ESP chip is selected or reselected by another initiator or target. The Enable Selection/Reselection command must have been issued before either sequence will be initiated. Bit 7 of the Enable Selection/Reselection command enables DMA during the Bus Initiated Sequences. If bit 7 is zero, any information transferred during one of these sequences will be stored in the FIFO. If bit 7 is a one, the information will be stored in memory using DMA.

These sequences reduce processor overhead by automating the processes and creating an interrupt only after a process is complete or an abnormal condition occurs.

The Select and Reselect command sequences automatically disable Bus Initiated selection/reselection after completing the selection or reselection. Normally, the microprocessor has 250 ms (the recommended select/reselect timeout) to issue the Enable Selection/Reselection command to the ESP chip after the chip disconnects from the bus. If this time is exceeded, an initiator or target which is attempting to select or reselect the ESP chip may timeout.

While a Bus Initiated Sequence is in progress, the command register is held reset. If a command is issued while a Bus Initiated sequence is in progress, the command will be ignored. If a Select or Reselect command was executing when the bus-initiated sequence began, the command will abort.

6.2.1 Selection

The Selection sequence will be performed when the Enable Selection/Reselection command has been issued and the chip is selected as a target by an initiator.

If the sequence completes normally, the following data will have been transferred from the initiator:

Selection bus ID	1 Byte
Identify message	1 Byte
Command descriptor block	6,10 or 12 Bytes

This data will be in the FIFO if the Enable Selection/Reselection command was issued without DMA enabled.

The selection bus ID byte is stored to enable the microprocessor to determine the initiator's ID. (The byte is not encoded). The absence of an initiator ID indicates that the system is in single-initiator mode.

The sequence terminates early if the received message byte is not an Identify message, if ATN is still asserted after the Identify message has been received, or if bad parity is received.

6.2.2 Reselection

The Reselection sequence will be performed when the Enable Selection/Reselection command has been issued and the chip is reselected as an initiator by a target.

If the sequence completes normally, the following data will have been transferred from the target:

Reselection bus ID	1 Byte
Message In (Identify)	1 Byte

The data will be in the FIFO if the Enable Selection/Reselection command was issued without DMA enabled.

The reselection bus ID byte is stored to enable the microprocessor to determine the target's ID. The byte is not encoded.

If the message byte was received, ACK will still be asserted on the SCSI bus and the host processor must issue a Message Accepted command to the ESP chip to release it. The host processor may reject the message by issuing the Assert ATN command prior to the Message Accepted command.

The sequence terminates early if Message In Phase was not asserted by the target.

6.2.3 SCSI Bus Reset

A SCSI bus reset may occur when the ESP is in any mode. The reset causes the ESP to disconnect from the SCSI bus and reset several internal states. (See Section 6.1)

If the SCSI reset interrupt has not been disabled in the configuration register, the ESP will set the interrupt bit and generate an interrupt to the microprocessor. If the interrupt is not serviced in approximately 1.7 ms, the ESP will assert the RESETO pin for 25 µs. (See Section 3.7, bit 7) It then loops back to wait another 1.7 ms for the interrupt to be serviced. This provides a watchdog timeout on the SCSI reset interrupt which can be used to reset the rest of the board in the event that the microprocessor is locked in an erroneous state.

If the SCSI bus reset is still active when the microprocessor clears the interrupt, a new interrupt will be generated which must be serviced.

6.3 Commands

The microprocessor issues commands to the ESP by writing to the dual-ranked Command Register. Caution should be exercised when overlapping commands to the ESP chip. Commands which transfer data in one direction should not be overlapped with commands that transfer data in the opposite direction. Also, for overlapped DMA commands, the transfer count must be loaded prior to loading the corresponding command. Care should be taken when overlapping non-DMA transmit commands, since many commands will completely empty the FIFO leaving nothing for the second command to transmit.

The 53C90 command set is divided into Disconnected, Target, Initiator, and Miscellaneous types:

6.3.1 Disconnected State Commands

The following commands are valid only when the 53C90 is in the disconnected state.

DISCONNECTED STATE COMMANDS		
Non-DMA	DMA	
40	C0	Reselect Sequence
41	C1	Select without ATN Sequence
41	C2	Select with ATN Sequence
42	C3	Select with ATN and Stop Sequence
44	C4	Enable Selection/Reselection
45	C5	Disable Selection/Reselection

If any of these commands are issued when the chip is not in a disconnected state, they will be ignored, the chip will generate an illegal command interrupt, and the Command Register will be cleared.

These sequences reduce processor overhead by automating the Selection or Reselection process. An interrupt is generated only after the entire sequence is complete or an abnormal condition occurs.

6.3.1.1 Reselect Sequence

This command will start the Reselect Sequence to connect the ESP as a target to an initiator.

Prior to issuing this command the microprocessor must set the timeout register, Select/Reselect bus ID registers and, if DMA is enabled, the Transfer Count Register must be set to 1. If DMA is not enabled, the message must be loaded into the FIFO prior to issuing this command to the ESP.

When the Reselect Sequence completes, the following data will have transferred to the Initiator:

Identify Message	1 byte

The sequence terminates early if a Reselect timeout occurs. This sequence does not use the Sequence Step Register.

6.3.1.2 Select without ATN Sequence

This command connects the chip as an initiator. A command block is sent to the target.

Prior to issuing this command the microprocessor must set the Timeout Register, Select/Reselect bus ID Registers and, if DMA is enabled, the Transfer Count Register must be set to the total length of the command. If DMA is not enabled, the data must be loaded into the FIFO prior to giving the command.

When this command completes normally, the following data will have transferred to the target:

Command Descriptor Block	6, 10, or 12 bytes

This command terminates early if:

- A select timeout occurs
- Target does not assert Command Phase
- Target removes Command Phase early

6.3.1.3 Select with ATN Sequence

The Select with ATN sequence command connects the chip as an initiator. A message and command block are sent to the target.

Prior to issuing this command the host processor must set the Timeout Register, Select/Reselect bus ID Registers and, if DMA is enabled, the Transfer Count Register must be set to the total length of the message and command. If DMA is not enabled, the data must be loaded into the FIFO prior to issuing this command.

The following data is transferred if Select with ATN completes normally:

Identify Message	1 byte
Command Descriptor Block	6, 10, or 12 bytes

The message can only be one byte in length. This command terminates early if:

- Select timeout occurs
- Target does not assert Message Out or Command Phase
- Target removes Command Phase early

6.3.1.4 Select with ATN and Stop Sequence

The Select with ATN and Stop sequence command should be used instead of the Select with ATN sequence if a message longer than one byte must be transferred. This command will start the Select sequence and stop after one message byte has been sent. ATN will remain asserted on the SCSI bus after the sequence completes. This allows the Initiator to send another message after the ID message has been sent.

This command terminates early if:

- Select timeout occurs
- Target does not assert Message Out Phase

This command is used to transfer extended messages such as Modify Data Pointers, Synchronous Data Transfer Requests and Extended Identify.

6.3.1.5 Enable Selection/Reselection

This command allows the ESP to respond to bus-initiated selection or reselection. Normally, this command is issued by the microprocessor to the ESP within 250ms (recommended select/reselect timeout) after the chip disconnects from the bus.

If DMA is enabled, the ESP will DMA the received data to buffer memory. If this bit is a zero, the received data will be left in the FIFO.

6.3.1.6 Disable Selection/Reselection

The Disable Selection/Reselection command disables the ESP from responding to bus-initiated selection or reselection. If the ESP has not yet begun a bus-initiated selection or reselection sequence, this command resets the internal mode bits which were previously set by the Enable Selection/Reselection command. The ESP then generates a function complete interrupt to the microprocessor.

If bus initiated selection or reselection has already begun, the Command Register is held reset so that all incoming commands are ignored. The ESP will generate selected or reselected interrupt when it completes.

6.3.2 Target Commands

The following commands are valid only when the chip is connected as a target.

TARGET COMMANDS		
Non-DMA	DMA	
20	A0	Send Message
21	A1	Send Status
22	A2	Send Data
23	A3	Disconnect Sequence
24	A4	Terminate Sequence
25	A5	Target Command Complete Sequence
27	A7	Disconnect
28	A8	Receive Message Sequence
29	A9	Receive Command
2A	AA	Receive Data
2B	AB	Receive Command Sequence

If any of these commands are issued when the chip is not in target mode, it will be ignored, the chip will generate an illegal command interrupt, and the Command Register will be cleared.

Prior to issuing a send command, if DMA is enabled, the transfer count must be set to the total number of bytes to be read from buffer memory. If DMA is not enabled, the data must be loaded into the FIFO. Prior to issuing a receive command, if DMA is enabled the Transfer Count must be loaded with the total number of bytes to transfer from the SCSI bus. If DMA is not enabled, only one byte will be received into the FIFO.

Normally, the commands terminate with a function complete interrupt. If ATN is asserted, the bus service interrupt is also set and the Command Register is cleared.

If ATN is asserted when the ESP is idle, a bus service interrupt is generated without the function complete bit set and the Command Register will be cleared.

6.3.2.1 Send Message (Message In Phase)

This command will change the phase lines to the Message In Phase and transmit bytes to the SCSI bus.

A function complete interrupt will be generated when the command is completed. If ATN is asserted during the execution of the command, the bus service interrupt will also be set, the Command Register will be cleared, and the command will terminate early.

6.3.2.2 Send Status (Status Phase)

This command will change the phase lines to the Status Phase and transmit bytes to the SCSI bus.

A function complete interrupt will be generated when the command is completed. If ATN is asserted during the execution of the command, the bus service interrupt will also be set, the Command Register will be cleared, and the command will terminate early.

6.3.2.3 Send Data (Data In Phase)

This command will change the phase lines to the Data In Phase and transmit bytes to the SCSI bus.

A function complete interrupt will be generated when the command is completed. If ATN is asserted during the execution of the command, the bus service interrupt will also be set, the Command Register will be cleared, and the command will terminate early.

6.3.2.4 Disconnect Sequence

This command will change the phase lines to the Message In Phase, send two message bytes to the initiator, and then disconnect from the SCSI bus. The Save Data Pointers and Disconnect messages will normally be sent. A function-complete and disconnect interrupt will be generated when the command is completed.

If ATN is asserted, the function complete and bus-service bits will be set, the Command Register is cleared, and the command will terminate early without disconnecting.

6.3.2.5 Terminate Sequence

This command will change the phase lines to the Status Phase and send one status byte, change to the Message In Phase and send one message byte, and then disconnect from the SCSI bus. This sequence is used to complete a command and will normally send the status followed by a Command Complete Message. A function complete and disconnect interrupt will be generated when the command is completed.

If ATN is asserted, the function-complete and bus-service bits will be set, the Command Register is cleared, and the command will terminate early without disconnecting.

6.3.2.6 Target Command Complete Sequence

This command will change the phase lines to the Status Phase and send one status byte, then change to the Message In Phase and send one message byte. This sequence is used to complete a linked command and will normally send the status followed by a Command Complete message. A function complete interrupt will be generated when the command is completed.

If ATN is asserted, the function-complete and bus-service bits will be set, the Command Register is cleared, and the command will terminate early without disconnecting.

6.3.2.7 Disconnect

This command releases all SCSI bus signals except RSTO and returns the ESP to a disconnected state (refer to the earlier initialization description). No interrupt is generated to the microprocessor.

6.3.2.8 Receive Message Sequence (Message Out Phase)

This command causes the ESP chip to change the phase lines to the Message Out Phase and receive bytes from the SCSI bus . The sequence generates a function complete interrupt when the command is completed. If ATN is still asserted, the bus service interrupt bit will also be set and the Command Register will be cleared.

If a parity error is detected, the ESP chip will receive message bytes and discard them until ATN is false. A function complete interrupt is generated, and the Command Register is cleared.

6.3.2.9 Receive Command (Command Phase)

This command will change the phase lines to the Command Phase and receives bytes from the SCSI bus . A function complete interrupt will be generated when the command is completed. Also, if bad parity was received during the transfer the Command Register will be cleared when the command completes.

If ATN is asserted during the execution of the command, the bus service interrupt will also be set, the Command Register will be cleared, and the command will terminate early.

6.3.2.10 Receive Data (Data Out Phase)

This command will change the phase lines to the Data Out Phase and receive bytes from the SCSI bus.

A function complete interrupt will be generated when the command is completed. Also, if bad parity was received during the transfer, the Command Register will be cleared.

If ATN is asserted during the execution of the command, the bus service interrupt will also be set, the Command Register will be cleared, and the command will terminate early.

6.3.2.11 Receive Command Sequence (Command Phase)

This command will change the phase lines to the Command Phase and receive bytes from the SCSI bus . The ESP examines the first byte received to determine the length of the command. If the length is unknown, the Transfer Counter will be loaded with 5 and the Transfer Complete bit in the Status Register will be cleared. Otherwise, the command is decoded, the Transfer Counter is loaded with the appropriate value (5, 9 or 11), and the Transfer Complete bit is set.

If bad parity is detected, the sequence will terminate early and the Command Register will be cleared. If ATN is set, the sequence does not terminate early but the bus service bit will be set and the Command Register will be cleared when the sequence completes.

6.3.3 Initiator Commands

The following commands are valid only when the chip is connected as an initiator. If any of these commands are issued when the chip is not in Initiator mode they will be ignored, the chip will generate an illegal command interrupt, and the Command Register will be cleared.

INITIATOR COMMANDS		
Non-DMA	DMA	
10	90	Transfer Information
11	91	Initiator Command Complete Sequence
12	92	Message Accepted
18	98	Transfer Pad

If BSY becomes false, the ESP generates a disconnect interrupt and returns to the disconnected state. (See section 6.1) Due to synchronization latency, a disconnect is detected by the ESP 1.5 to 3.5 cycles after it actually occurs on the bus.

Prior to issuing a command to send data to the SCSI bus, if DMA is enabled the transfer count must be set to the total number of bytes to read from buffer memory. If DMA is not enabled, the data must be loaded into the FIFO.

Prior to issuing a command to receive data from the SCSI bus, if DMA is enabled the transfer count must be loaded with the total number of bytes to transfer from the SCSI bus. If DMA is not enabled, only one byte will be accepted by the FIFO.

Received bytes are checked for parity if the parity enable bit is set in the Configuration Register. If a parity error is detected, the chip asserts ATN prior to deasserting ACK for the byte which was error. It also sets the parity error status bit.

6.3.3.1 Transfer Information

The Transfer Information command is used to perform general transfers over the SCSI bus while in initiator mode. The ESP will continue to Transfer Information until one of four terminating events occurs:

- The transfer is complete. If the phase is Message Out, the chip removes ATN prior to asserting ACK for the last byte of the message. When the target asserts REQ, a bus service interrupt is generated.

- The target changes the information phase before the expected number of bytes was transferred. The ESP clears the Command Register and generates a bus service interrupt when REQ is asserted by the target.

- The target releases BSY, which generates a disconnect interrupt and a disconnect reset (refer to the earlier initialization description).

- The chip receives the last byte of a Message In Phase. The chip leaves ACK asserted and generates a function complete interrupt.

A Transfer Information command to transfer synchronous data must use DMA. Synchronous data in transfers are unique in that the target may at any time send data and REQ pulses to the initiator. These bytes must be stored in the FIFO as they are sent. Initiator transfers are handled internally as follows:

- All Message In and Status Phase transfers are handled one byte at a time If DMA is enabled, the next byte will not be received until the current byte has been written to buffer memory and the FIFO is empty.

If the phase changes to Synchronous Data In, the DMA interface is immediately disabled to ensure that no data bytes are transferred to buffer memory. Also, if bad parity is detected on the incoming data bytes, it is not immediately reported. This is because the status register must reflect the status of the completing command, not the new data. The status bit and ATN are set when the next Transfer Info command begins executing.

- All Message Out and Command Phase transfers are handled one byte at a time. If DMA is enabled, the DMA interface only issues one DMA request at a time. If the phase changes to synchronous Data In, the DMA interface is already inactive so no extra bytes will be loaded into the FIFO.

If DMA is not enabled and the phase changes to Synchronous Data In, there may be bytes remaining in the FIFO which have not yet been transmitted. The FIFO flags register is latched to indicate the number of non-data bytes that were in the FIFO, and then the FIFO is flushed of these bytes. The FIFO will contain only the incoming data bytes.

- In synchronous Data Out Phase, the offset counter is incremented as REQ pulses are received. The transfer completes when the FIFO is empty and the transfer counter is zero. The offset counter may or may not be zero, depending on whether the target continues requesting synchronous data.

- In synchronous Data In Phase, the transfer counter is clocked by the DMA interface as bytes are unloaded from the FIFO, rather than being clocked as bytes are loaded into the FIFO. The transfer completes when the transfer counter is zero. The FIFO may or may not be empty, depending on whether the target continues sending synchronous data.

6.3.3.2 Initiator Command Complete Sequence

This command will normally be issued when a status phase is received. If the sequence completes normally, the following data will have been transferred from the target:

Status	1 Byte
Message In	1 Byte

The data will be in the FIFO if the command was not issued with DMA enabled.

The sequence terminates early if the target does not assert the Message In Phase or if it disconnects. This sequence does not utilize the Sequence Step Register.

6.3.3.3 Message Accepted

The Message Accepted command releases the ACK signal. Upon completion of this command, the chip waits for the target to assert REQ and then generates a bus service interrupt.

When the chip receives the last byte of a message, it leaves the ACK signal asserted so that ATN can be asserted with the Set ATN command if the message is to be rejected. The Message Accepte command must always be issued to release ACK if it was left asserted whether or not ATN is asserted.

6.3.3.4 Transfer Pad

The Transfer Pad command is similar to the Transfer Information command, except that the information being transferred is null data. For an output transfer, the ESP uses the FIFO to generate pads for the SCSI bus. For an input transfer, the ESP receives data from the SCSI bus into the top of the FIFO without checking parity, and then discards it from the bottom of the FIFO.

A Transfer Pad command to transmit pad bytes must have DMA enabled. No DMA requests are actually made, but the ESP uses the Transfer Counter to determine when the transfer is complete.

The command terminates under the same conditions as the Transfer Information command, except that the chip does not leave ACK asserted on the last byte of a message in phase. If the command terminates early (due to a phase change or a disconnect), the FIFO may contain pad bytes.

6.3.3.5 Set ATN

The Set ATN command causes the ATN signal to be asserted. No interrupt is generated upon completion of this command.

The ESP automatically asserts the ATN signal for the following cases:

- A Select with ATN command is issued and arbitration is won.
- A parity error is detected on a byte received in initiator mode. ATN is asserted prior to releasing ACK.

The ESP automatically releases the ATN signal during the last byte of the Transfer Information command for a Message Out Phase. ATN is released prior to asserting the ACK signal.

6.3.4 Miscellaneous Commands

Miscellaneous Commands described in this section are valid in all modes. These commands do not check for ATN. If the ESP is a Target device and ATN happens to be asserted during the execution of one of these commands no bus service interrupt will be generated. It will be reported on completion of the next Target command, if the chip does not become disconnected.

MISCELLANEOUS COMMANDS		
Non-DMA	DMA	
00	80	NOP
01	81	Flush FIFO
02	82	Reset Chip
03	83	Reset SCSI Bus

6.3.4.1 NOP Command

The NOP command performs no operation. It is also used following a Reset Chip command to free the ESP Command Register. No interrupt is generated on completion of this command.

6.3.4.2 Flush FIFO Command

The Flush FIFO command initializes the FIFO to the empty condition. No interrupt is generated on completion of this command.

6.3.4.3 Reset Chip Command

The Reset Chip command resets all functions in the chip and returns it to a disconnected state. The command has the same effect as a hardware reset (refer to the earlier initialization description).

The Reset Chip command will remain in the top of the Command Register (locking the ESP and its registers in a reset state) until a new command is loaded. The new command must be a NOP command. This command might not be readable or executable.

6.3.4.4 Reset SCSI Bus Command

The Reset SCSI Bus command asserts the SCSI RSTO pin for 25µs (see section 3.7, bit 7). The chip is returned to a disconnected state. No interrupt is generated on completion of this command. Since the RSTI pin will be externally connected to the RSTO pin, an SCSI reset interrupt will be generated if it is not disabled in the Configuration Register.

6.3.5 Illegal Command

An illegal command is a command that is not allowed in the current ESP mode as specified by bits 6-4 of the Command Register or is an unsupported command as determined by bits 3-0. The chip will generate an illegal command interrupt to the microprocessor and clear the Command Register when an illegal command occurs.

An illegal command interrupt will also be generated if an initiator Transfer Information, Transfer Pad, or Command Complete command is issued when ACK is still asserted. Also, an illegal command interrupt is generated when a Select or Reselect command is issued with DMA if the Enable Selection/Reselection command was previously issued with DMA enabled.

To determine if an illegal command was written to the chip, check for the occurrance of an interrupt (i.e. INT/ active) and bit 6 of the Interrupt Status Register (register 5) being set.

7. SEQUENCE STEPS AND FLOW CHARTS

7.1 Sequence Steps

7.1.1 Bus Initiated Selection with ATN (Target)

Bus Initiated Selection with ATN (Target)		
SEQ STEP 2 1 0	INT REG 7 6 5 4 3 2 1 0	DESCRIPTION
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, received bus ID and one message byte. Check parity bit in Status Register.
0 0 0	0 0 0 1 0 0 1 0	Same as above; ATN on
0 0 1	0 0 0 0 0 0 1 0	Command Phase; all bytes not received because of parity error. Check Transfer Complete bit in Status Register. Check FIFO Flags/Counter.
0 0 1	0 0 0 1 0 0 1 0	Same as above; ATN on
0 1 0	0 0 0 0 0 0 1 0	Command Phase completed. Check transfer complete bit in Status Register
0 1 0	0 0 0 1 0 0 1 0	Same as above; ATN on

7.1.2 Bus Initiated Selection (Target)

Bus Initiated Selection (Target)		
SEQ STEP 2 1 0	INT REG 7 6 5 4 3 2 1 0	DESCRIPTION
0 0 0	0 0 0 0 0 0 0 1	Selected; received Initiator ID
0 0 1	0 0 0 0 0 0 0 1	Command Phase; all bytes not received because of parity error. Check FIFO Flags/ Counter.
0 0 1	0 0 0 1 0 0 0 1	Same as above; ATN on
0 1 0	0 0 0 0 0 0 0 1	Command Phase completed. Check Transfer Complete bit in Status Register.
0 1 0	0 0 0 1 0 0 0 1	Same as above; ATN on

7.1.3 Select with ATN (Initiator)

Select with ATN (Initiator)		
SEQ STEP 210	INT REG 76543210	DESCRIPTION
000	00100000	Arbitration completed; selection timeout; Disconnected
000	00011000	Arbitration and select completed. Not Message Out Phase; ATN on
010	00011000	Arbitration and Select completed; Message Out Phase; sent one byte. ATN off; Not Command Phase
011	00011000	Command Phase. All command bytes not transferred because of premature phase change
100	00011000	Select with ATN completed, not Command Phase

7.1.4 Select with ATN and Stop (Initiator)

Select with ATN and Stop (Initiator)		
SEQ STEP 210	INT REG 76543210	DESCRIPTION
000	00100000	Arbitration completed; Selection timeout; disconnected.
000	00011000	Arbitration and Select completed. Not Message Out Phase; ATN on
001	00011000	Sent one message byte, ATN on

7.1.5 Select without ATN (Initiator)

Select without ATN (Initiator)		
SEQ STEP 210	INT REG 76543210	DESCRIPTION
000	00100000	Arbitration complete; Select timeout. Disconnected
010	00011000	Arbitrate and Select completed. Not Command Phase.
011	00011000	Aribtrate and Select completed. Command Phase; all command bytes not transferred because of Phase change.
100	00011000	Arbitrate, Select, and Command Phase completed.

7.1.6 Receive Command Sequence (Target)

Receive Command Sequence (Target)		
SEQ STEP 210	INT REG 76543210	DESCRIPTION
001	00001000	Command Phase set; all bytes not received because of parity error. Check FIFO Flags/ Counter. Check Transfer Complete bit.
001	00011000	Same as above; ATN on.
010	00001000	Command Sequence completed. Check Transfer Complete bit.
010	00011000	Same as above; ATN on.

7.1.7 Command Complete Sequence (Target)

Command Complete Sequence (Target)		
SEQ STEP 210	INT REG 76543210	DESCRIPTION
000	00011000	Status phase, sent one byte; ATN on.
001	00011000	Status Phase completed. Message In Phase; sent one byte; ATN on.
010	00001000	Command Complete Sequence completed.

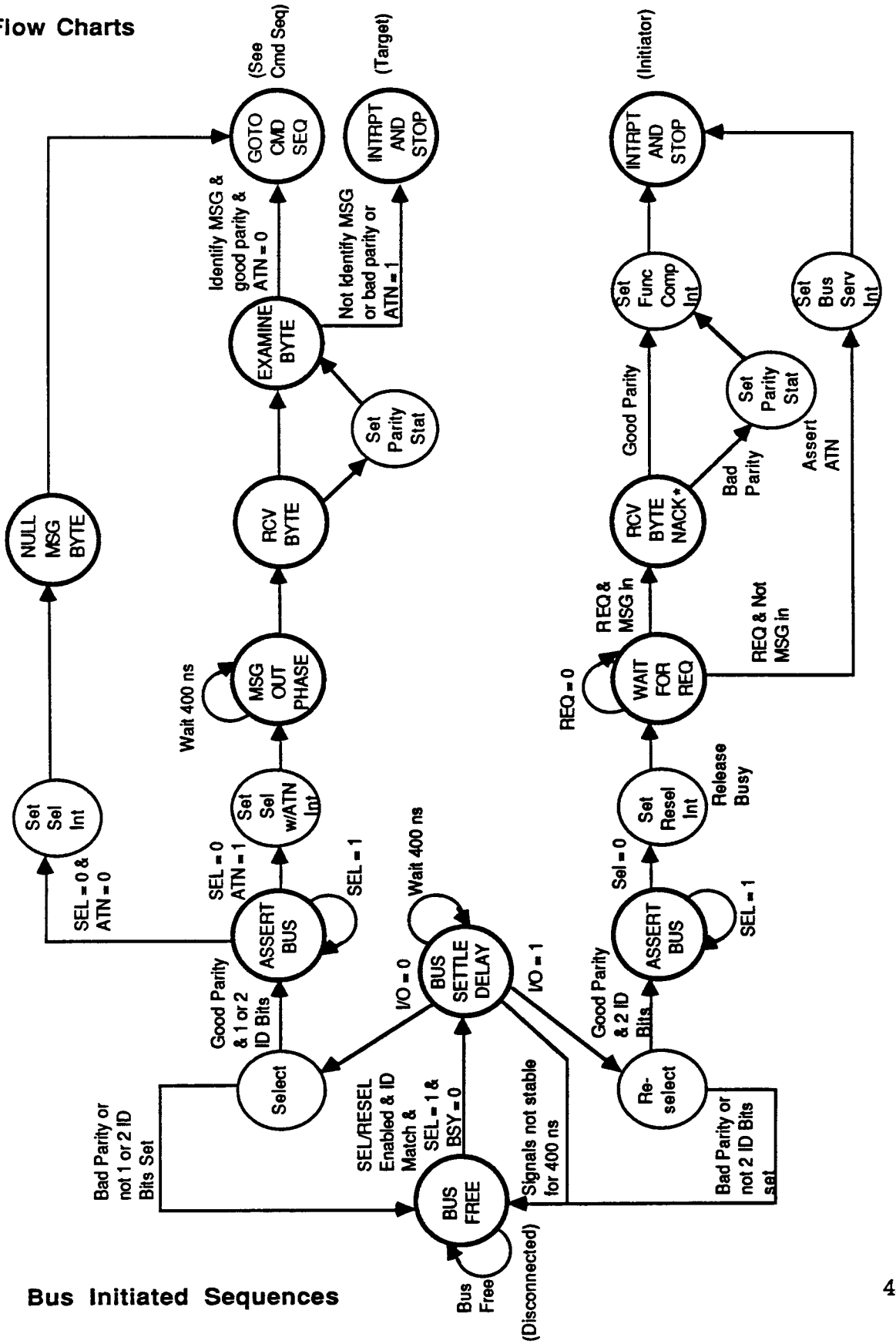
7.1.8 Disconnect Sequence (Target)

Disconnect Sequence (Target)		
SEQ STEP 210	INT REG 76543210	DESCRIPTION
000	00011000	Message In Phase; sent one byte; ATN on.
001	00011000	Message In Phase; sent second byte; ATN on.
010	00101000	Disconnect Sequence completed.

7.1.9 Terminate Sequence (Target)

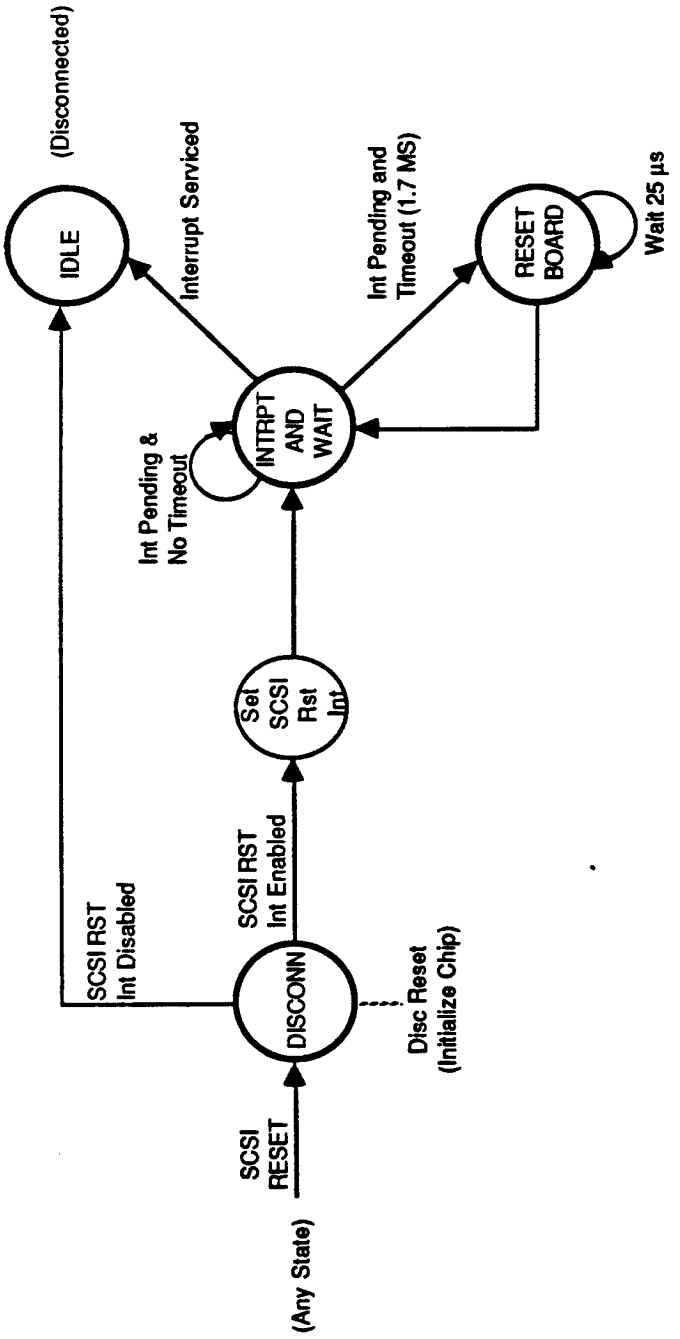
Terminate Sequence (Target)		
SEQ STEP 210	INT REG 76543210	DESCRIPTION
000	00011000	Status Phase, sent one byte; ATN on.
001	00011000	Status complete. Message In Phase, sent one byte; ATN on.
010	00101000	Terminate Sequence Completed.

7.2 Flow Charts



*Note: NACK = ACK remains asserted until Message Accepted issued.

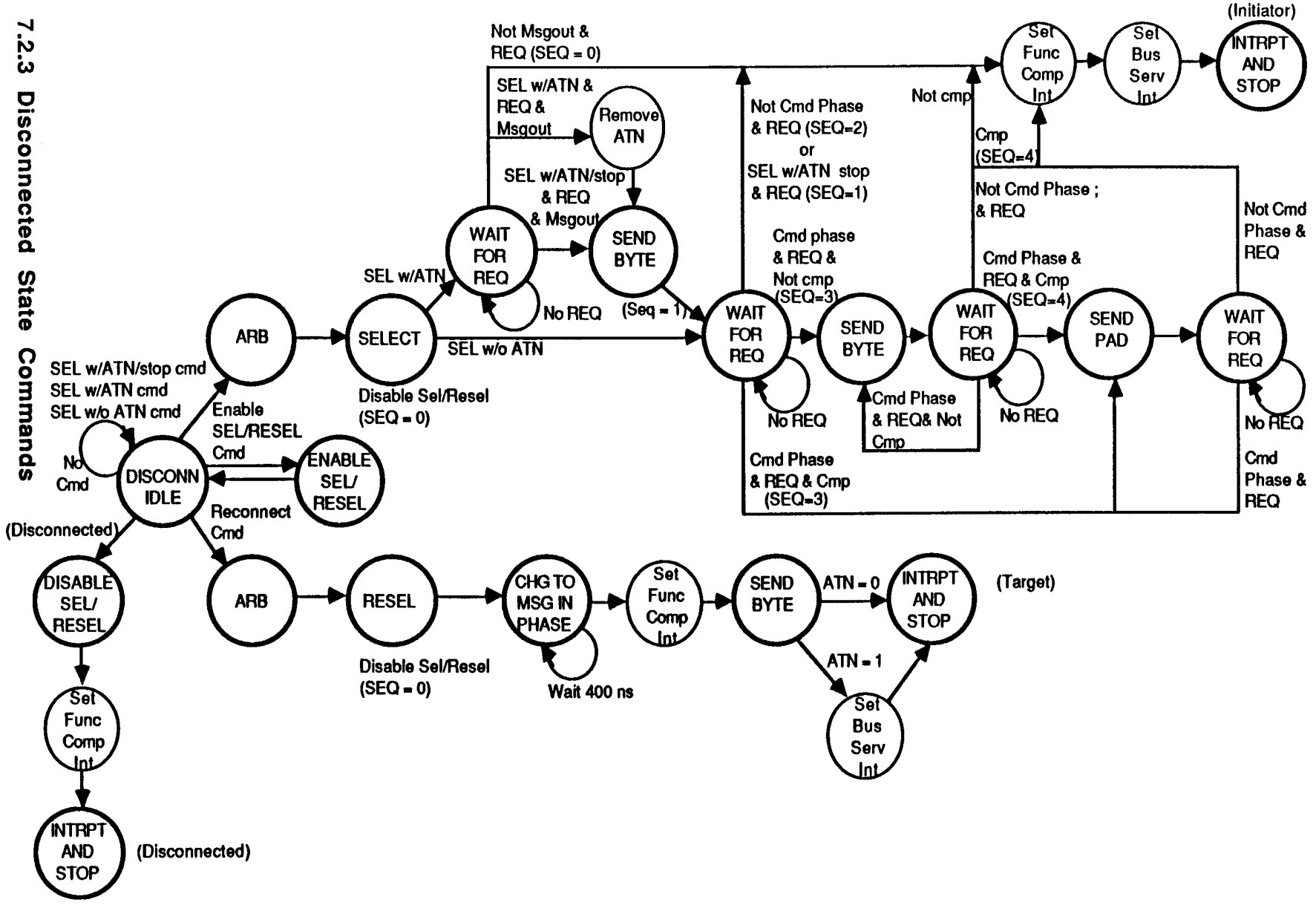
7.2.1 Bus Initiated Sequences



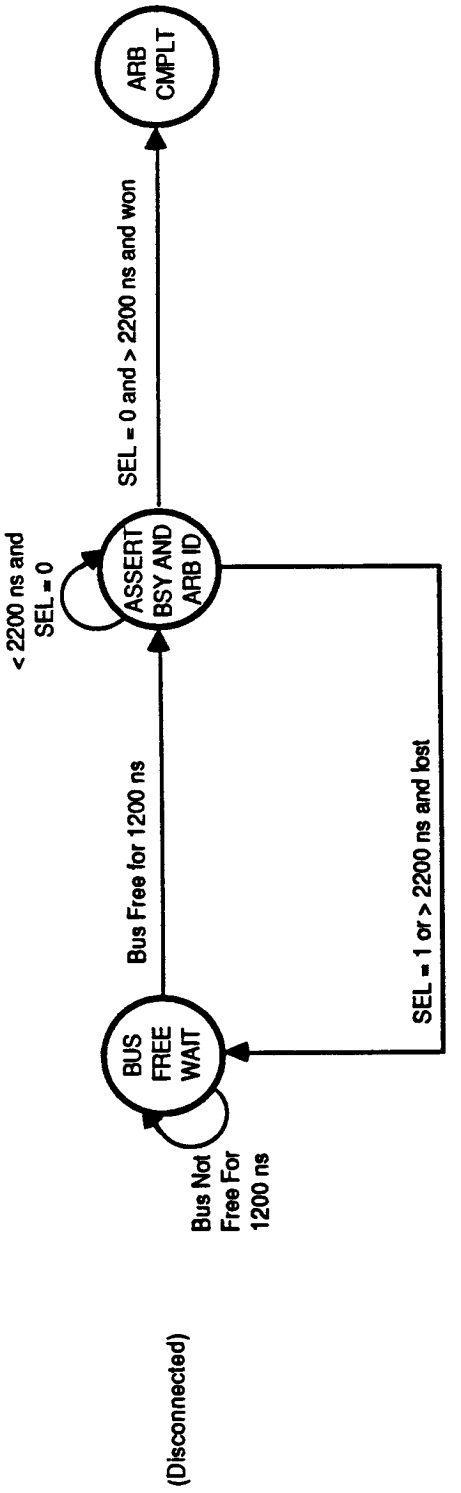
7.2.2 SCSI Reset

Bus Initiated Sequences

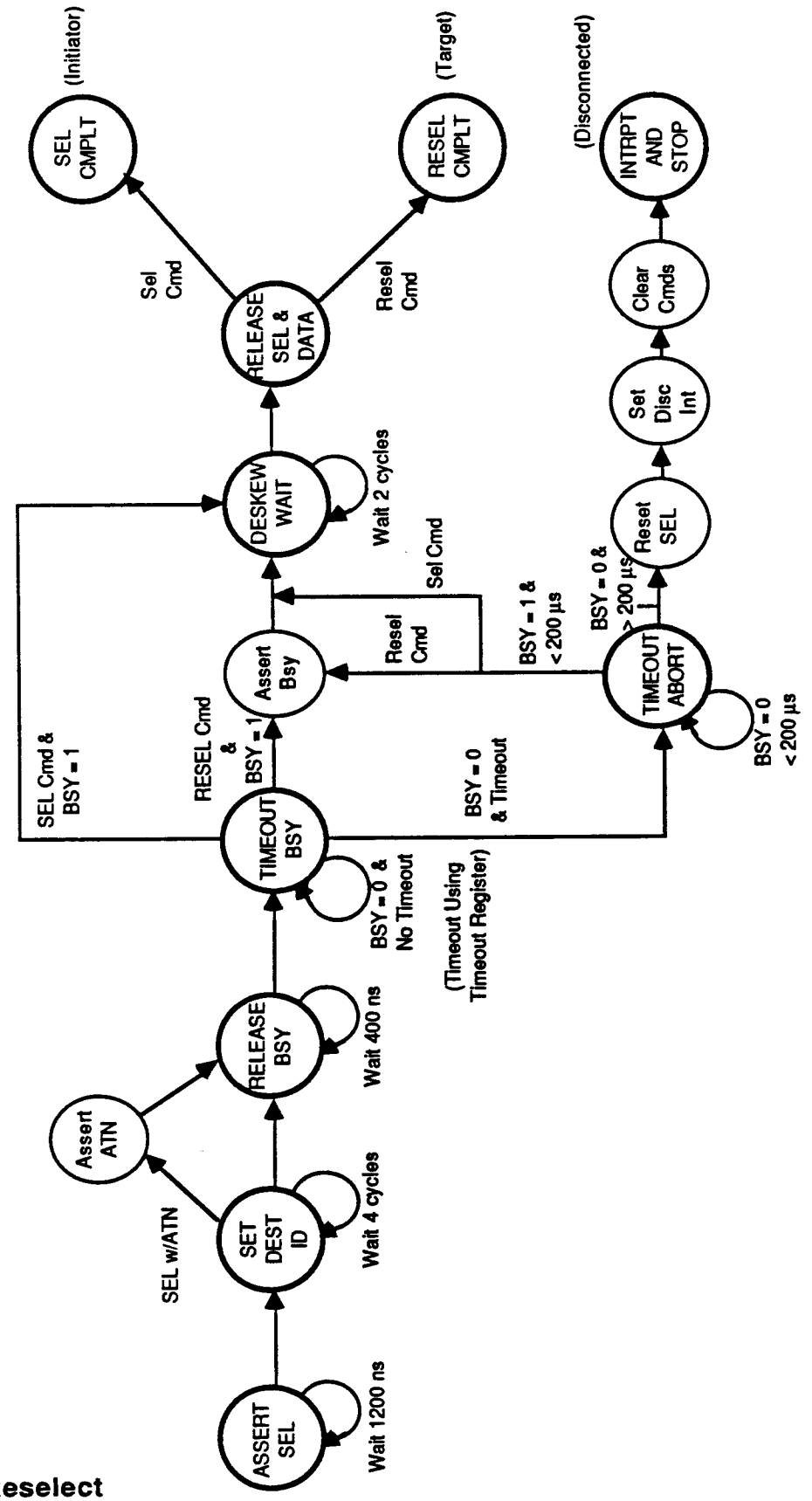
7.2.3 Disconnected State Commands



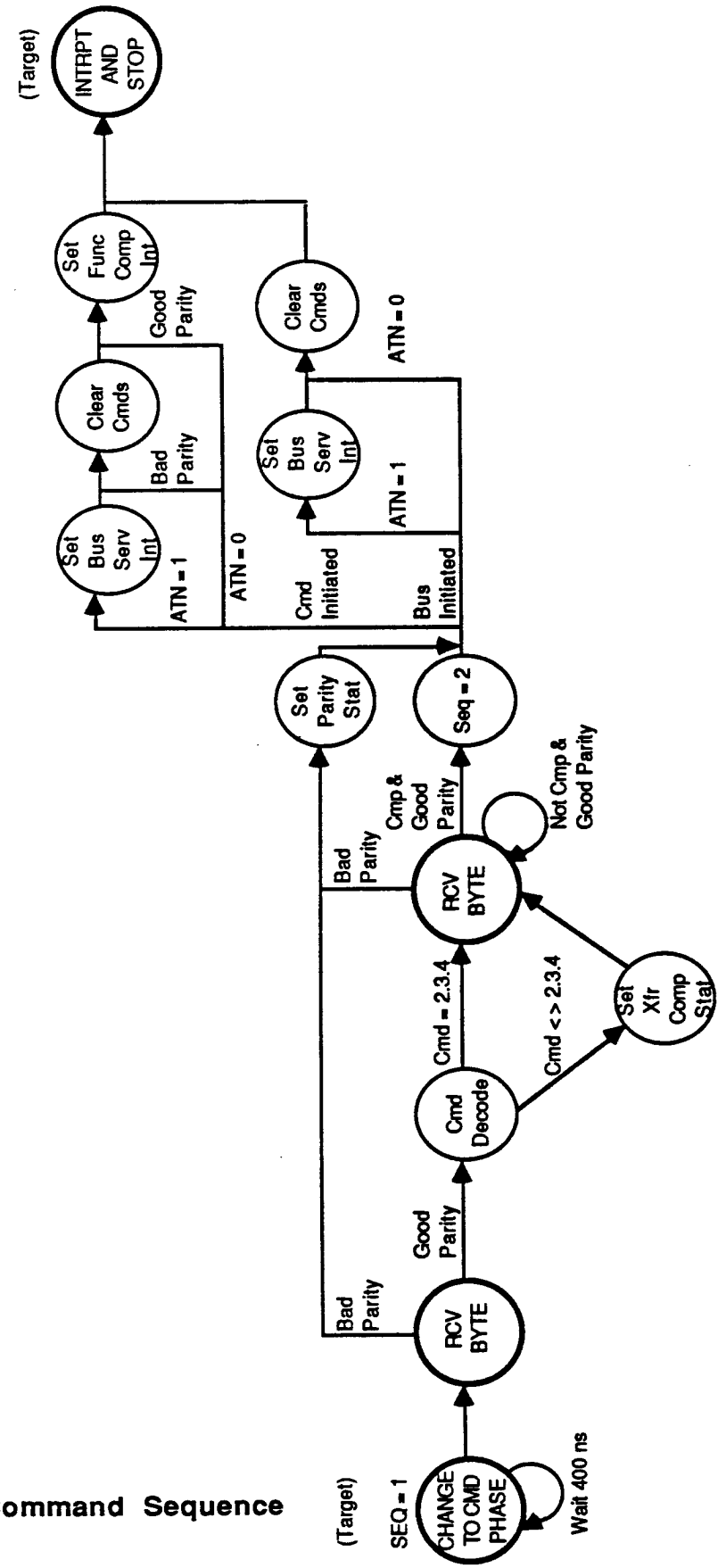
Disconnected State Commands (cont.)



7.2.4 Arbitrate

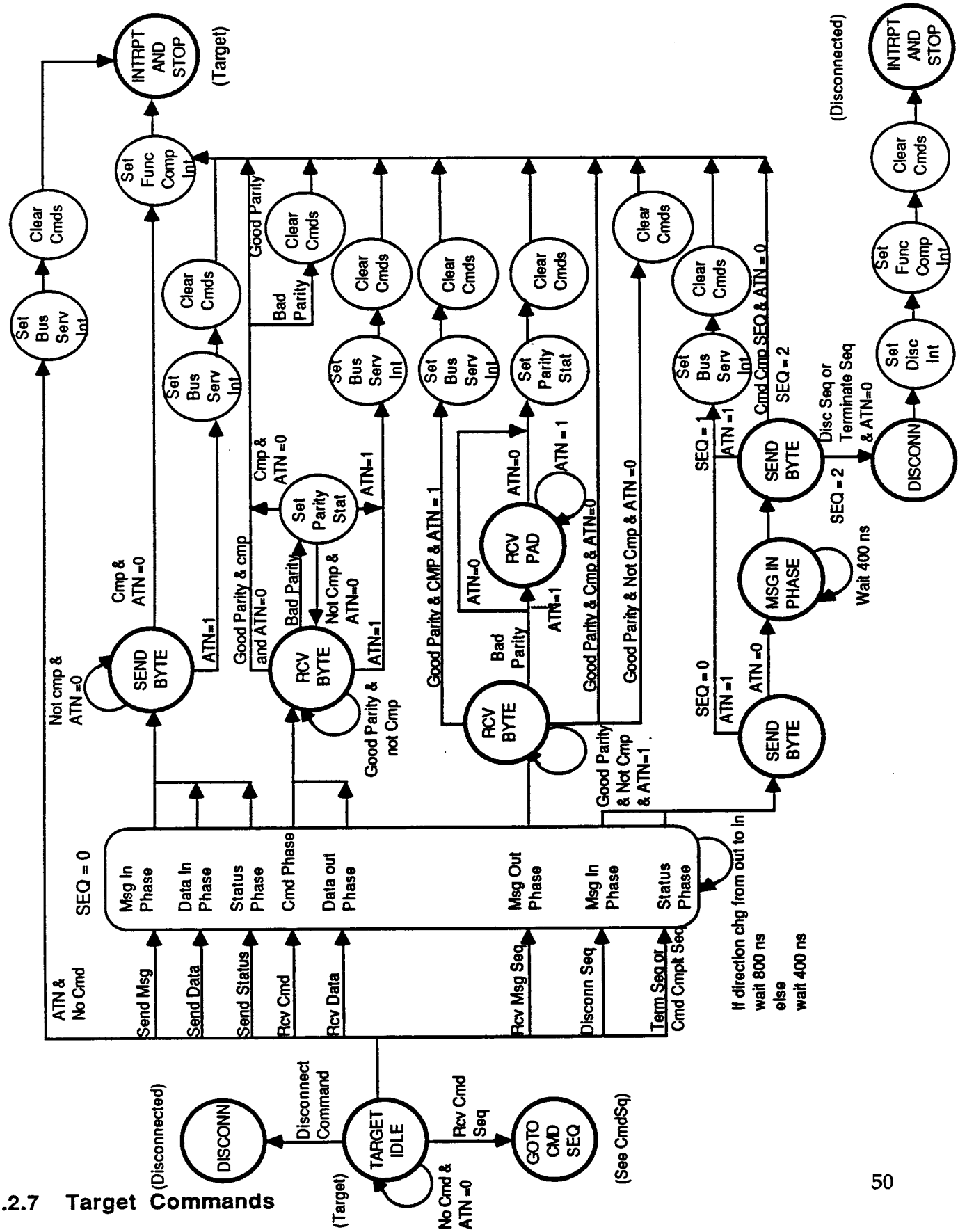


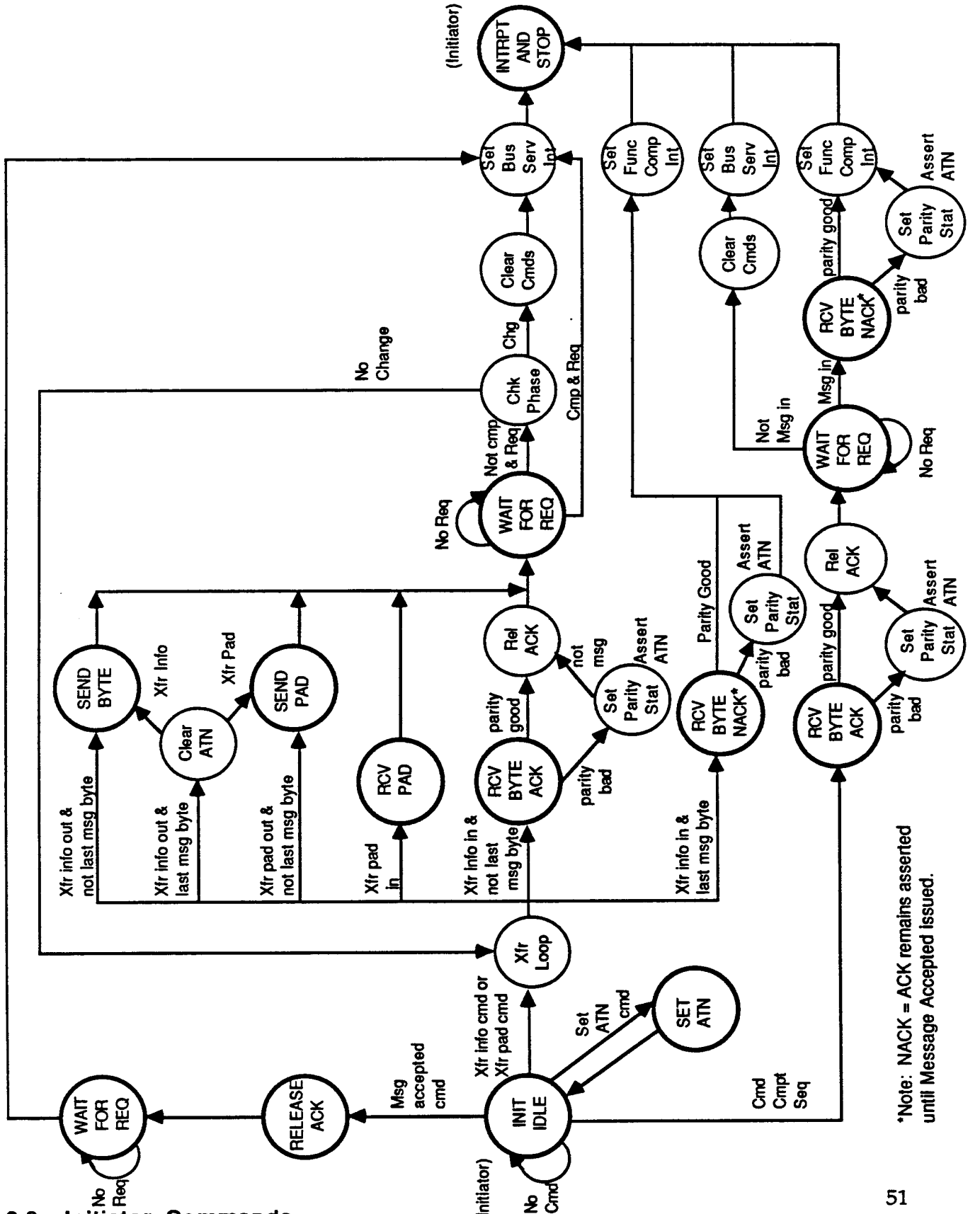
7.2.5 Select/Reselect



7.2.6 Command Sequence

7.2.7 Target Commands





7.2.8 Initiator Commands

8. ELECTRICAL CHARACTERISTICS

8.1 D.C. Characteristics

8.1.1 Absolute Maximum Stress Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tstg	Storage Temperature	-55	150	°C
VDD	Supply Voltage	-0.5	7.0	V
VIN	Input Voltage	VSS - 0.5	VDD + 0.5	V
ESD*	Electrostatic Discharge (All except SCSI pins)	-4000	4000	V
ESD*	Electrostatic Discharge (SCSI pins)	-7000	7000	V

*Test using the human body model--100pF at 1.5kΩ

8.1.2 Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply Voltage	4.75	5.25	V
IDD*	Supply Current (Static IDD)	0	10	mA
IDD	Supply Current	0	50	mA

Data Bus Lines DB0 - DB7

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	VSS - 0.5	0.8	V	
IIL	Input Leakage Current		-400	10	μA 0 < VIN < VDD
VOH	Output High Voltage	2.4	VDD	V	IOH = -400 μA
VOL	Output Low Voltage	VSS	0.4	V	IOL = 2 mA

CLK, RESET, A3-A0

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	VSS - 0.5	0.8	V	
IIL	Input Leakage Current	-10	10	µA	0 < VIN < VDD

CS/, RD/, WR/, ACK/, DIFFM

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIH	Input High Voltage	2.2	VDD + 0.5	V	

DREQ, TGS, IGS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VOH	Output High Voltage	2.4	VDD	V	IOH = -400 µA
VOL	Output Low Voltage	VSS	0.4	V	IOL = 2 mA
IOZ	Tri-State Leakage Current	-10	10	µA	0 < VOUT < VDD

INT/

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VOL	Output Low Voltage	VSS	0.4	V	IOL = 2 mA
IOZ	Tri-State Leakage	-10	10	µA	0 < VOUT < VDD

RSTI/, SELI/, BSYI/, ATNI/, MSGI/, CDI/, IOI/, REQI/, ACKI/

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIL	Input Low Voltage	VSS - 0.5	0.8	V	
VIH	Input High Voltage	2.0	VDD + 0.5	V	
IIL	Input Leakage Current	-10	10	µA	0 < VIN < VDD

RSTO/, SELO/, BSYO/, ATNO/, MSGO/, CDO/, IOO/, REQO/, ACKO/, SDO0-SDO7/, SDOP/

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VOL	Output Low Voltage	VSS	0.5	V	IOL = 48 mA
IOZ	Tri-State Leakage Current	-10	10	µA	0 < VOUT < VDD
SFT	Signal Fall Time	4 8		ns	IOL = 48 mA

RESETO

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VOH	Output High Voltage	2.4	VDD	V	IOH = -4 mA
VOL	Output Low Voltage	VSS	0.4	V	IOL = 4 mA
IOZ	Tri-State Leakage	-10	10	µA	0 < VOUT < VDD

SDI0-SDI7/

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIL	Input Low Voltage	2.0	VDD + 0.5	V	
VIH	Input High Voltage	VSS - 0.5	0.8	V	
HST	Hysteresis	200		mV	
IIL	Input Leakage Current	-10	10	µA	0 < VIN < VDD
VOH	Output High Voltage	2.4	VDD	V	IOH= -400 µA
VOL	Output Low Voltage	VSS	0.4	V	IOL = 2 mA

8.2 A.C. Characteristics

The A.C. characteristics described in this section apply over the voltage range Vdd equal to 4.75 to 5.25 volts and the temperature range 0 to 70°C. Chip output timing is based on simulation under worst case conditions (4.75 V, 70°C) and the following pad termination:

SYMBOLS	OUTPUT LOADS	
RESETO, DREQ	50 pf	
DB7...0	85 pf	
TGS, IGS	50 pf	
SDIP/, SDI7/..0	50 pf	
INT/	50 pf	1K pullup
RSTO/, SELO/, BSYO/, ATNO/, MSGO/, CDO/ IOO/, REQO/, ACKO/, SDO7...0/, SDOP/	200 pf	110 pullup 165 pulldown

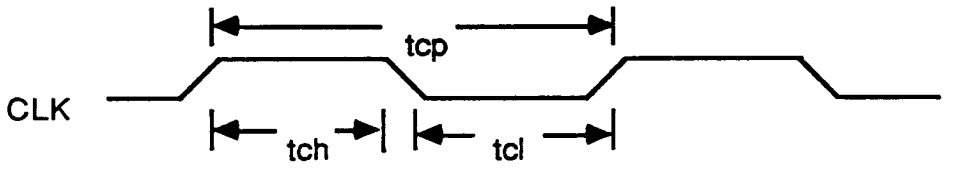
8.2.1 System Interface

All timings in this specification are taken from the 10% & 90% points with respect to the specified VOL & VOH of the waveforms.

8.2.1.1 Clock Interface

Symbol	Description	Min	Max	Unit
tcp	Clock period	40	100	ns
fcpa	Clock frequency, async	10*	25	MHz
fcps	Clock frequency, sync	13*	25	MHz
tch	Clock high	.45 tcp	.55 tcp	ns
tcl	Clock low	.45 tcp	.55 tcp	ns

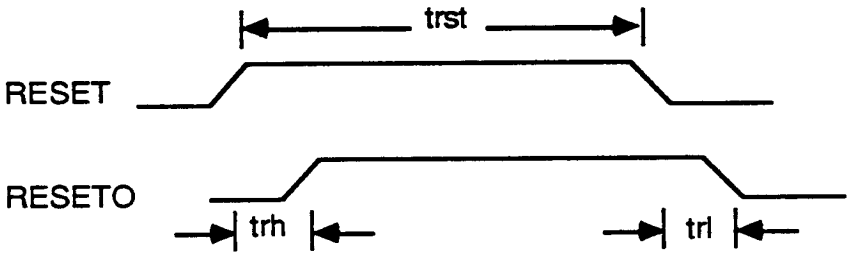
*Note: These minimum numbers required to comply with ANSI SCSI specification.



8.2.1.2 Reset Input

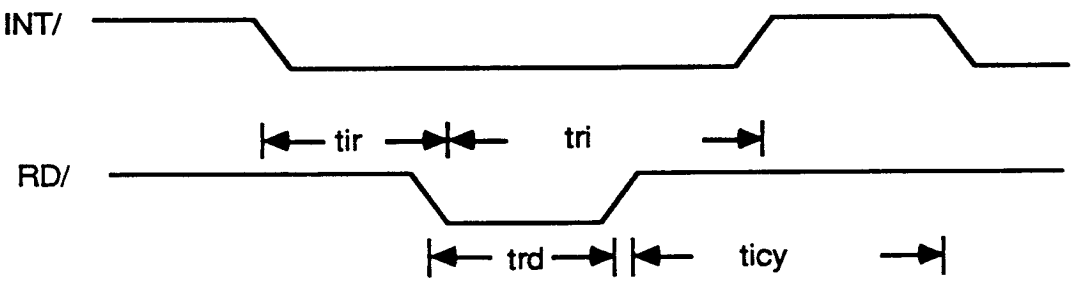
Symbol	Description	Min	Max	Unit
trst	Reset pulse width	*2tcp or 200		ns
trh	Reset high to RESETO high		50	ns
trl	Reset low to RESETO low		50	ns

* Whichever is longer



8.2.1.3 Interrupt Output

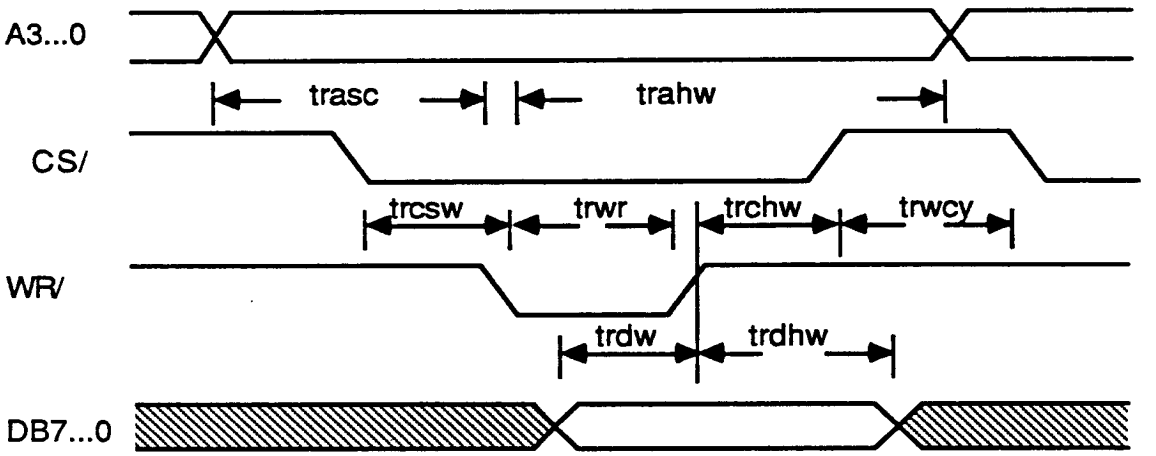
Symbol	Description	Min	Max	Unit
tir	INT/ to RD/	2tcp		ns
trd	RD/ pulse width	50		ns
tri	RD/ low to INT/ high		70 +3.6tcp	ns
ticy	RD/ high to INT/ low	1.4 tcp		ns



8.2.2 Register Interface

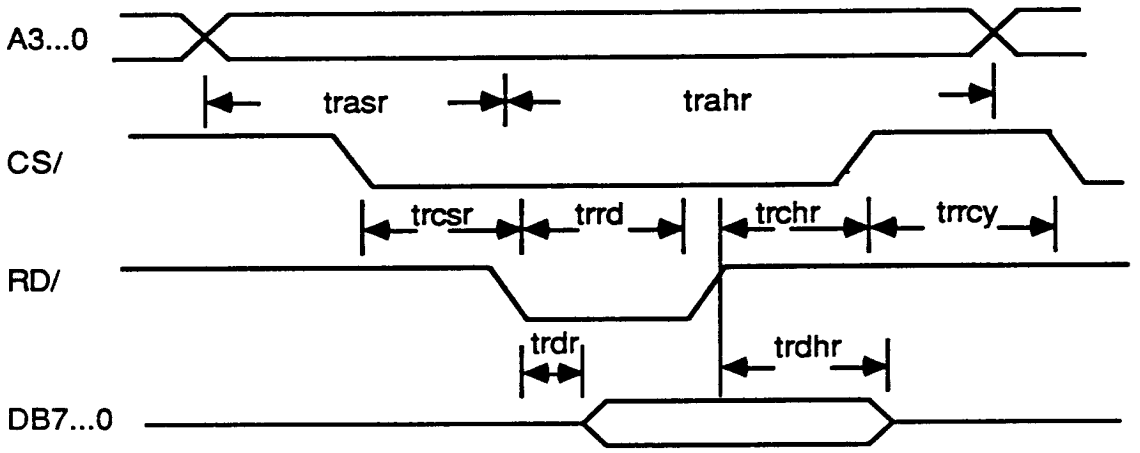
8.2.2.1 Register Write

Symbol	Description	Min	Max	Unit
trasc	Address setup to WR/	12		ns
trcsw	CS/ setup to WR/	12		ns
trwr	WR/ pulse width	40		ns
trdw	Data to WR/ high	20		ns
trahw	Address hold time from WR/	30		ns
trdhw	Data hold time	10		ns
trchw	WR/ high to CS/ high	12		ns
trwcy	CS/ high to CS/ low	60		ns



8.2.2.2 Register Read

Symbol	Description	Min	Max	Unit
trasr	Address setup to RD/	12		ns
trcsr	CS/ setup to RD/	12		ns
trrd	RD/ pulse width	2tcp		ns
trdr	RD/ to data		50	ns
trahr	Address hold time from RD/	30		ns
trdhr	Data hold time	2	50	ns
trchr	RD/ high to CS/ high	12		ns
trrcy	CS/ high to CS/ low	30		ns

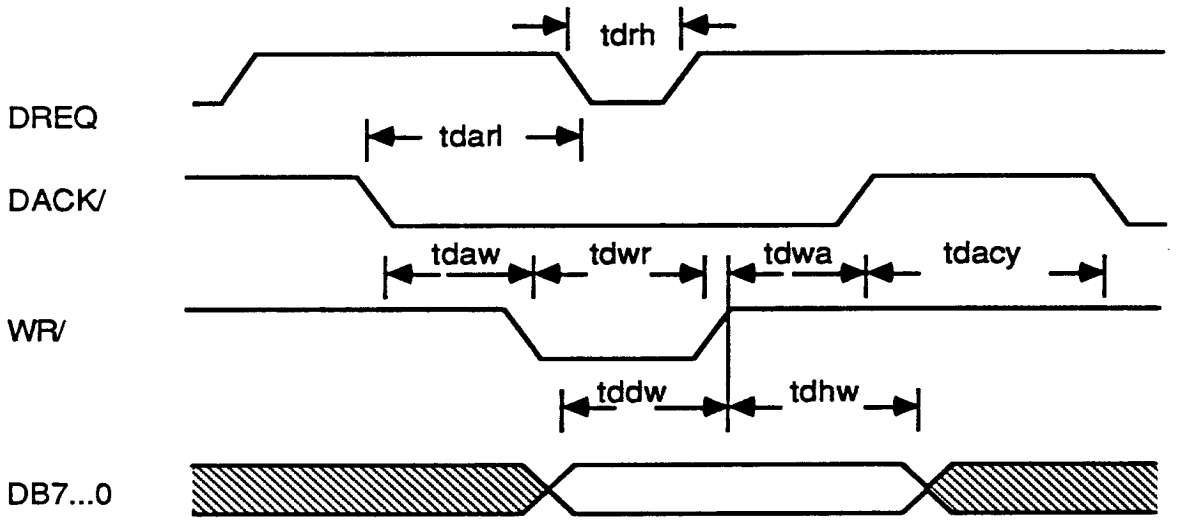


8.2.3 DMA Interface

8.2.3.1 DMA Write

Symbol	Description	Min	Max	Unit
tdarl *(1)	DACK/ low to DREQ low	0	65	ns
tdaw	DACK/ low to WR/ low	0		ns
tdwr	WR/ pulse width	40		ns
tddw	Data to WR/ high	20		ns
tdwa *(1,2)	WR/ high to DACK/ high	12		ns
tdhw	Data hold time	10		ns
tdacy *(1,2)	DACK/ high to DACK/ low	12		ns
tdrh	DREQ low to DREQ high	0		ns

*Notes: 1. If tdacy + tdwa ≥ 30 ns, tdarl = 60 ns maximum
2. If tdacy ≥ 20 ns, tdwa = 0 ns minimum



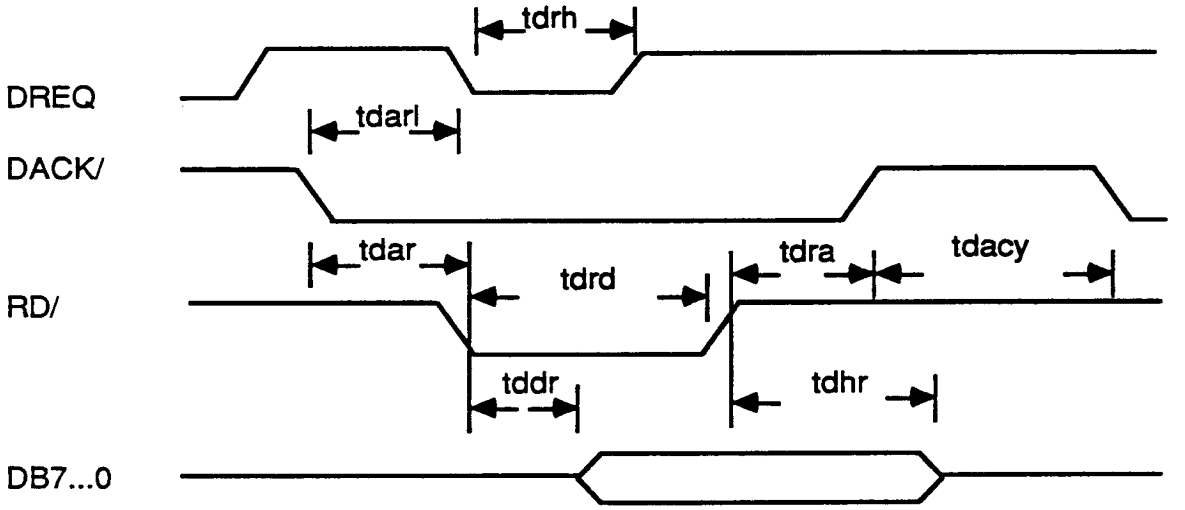
- For synchronous data transfers DACK/ low to DACK/ high must equal tcp + 20 ns minimum.

- DREQ will remain active as long as the FIFO is not full and the transfer counter is not zero.

8.2.3.2 DMA Read

Symbol	Description	Min	Max	Unit
tdarl	DACK/ low to DREQ low	0	65	ns
tdar *(1,2)	DACK/ low to RD/ low	12		ns
tdrd	RD/ pulse width	50		ns
tddr *(1)	RD/ to data		50	ns
tdra	RD/ high to DACK/ high	0		ns
tdhr	Data hold time	2	50	ns
tdacy *(1,2)	DACK/ high to DACKN/low	12		ns
tdrh	DREQ low to DREQ high	0		ns

*Notes: 1. If tdacy + tdar ≥ 30 ns, tddr = 45 ns maximum
2. If tdacy ≥ 20 ns, tdar = 0 ns minimum



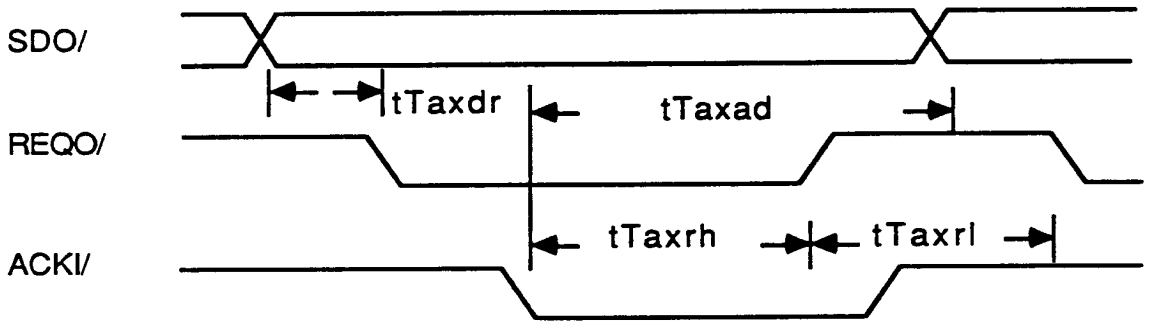
- For synchronous data transfers DACK/ low to DACK/ high must equal tcp + 20 ns minimum.

- DREQ will remain active as long as the FIFO has data to be read and the transfer counter is not zero.

8.2.4 Target Asynchronous Transfers

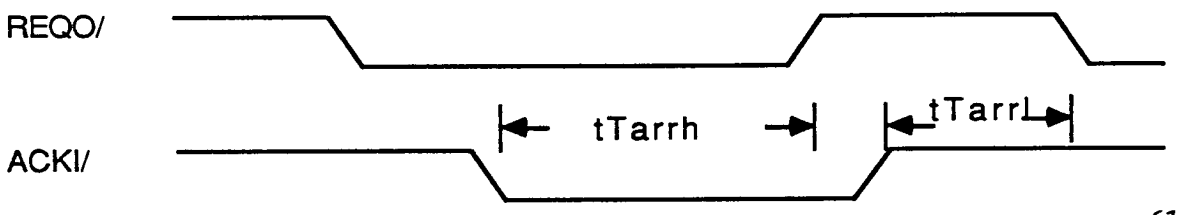
8.2.4.1 Target Asynchronous Send

Symbol	Description	Min	Max	Unit
tTaxdr	Data to REQO/ low	55		ns
tTaxrh	ACKI/ low toREQO/ high		49	ns
tTaxad	ACKI/ low to data (FIFO bottom full)		83	ns
tTaxrl	ACKI/ high to REQO/ low (data already set up)		54	ns



8.2.4.2 Target Asynchronous Receive

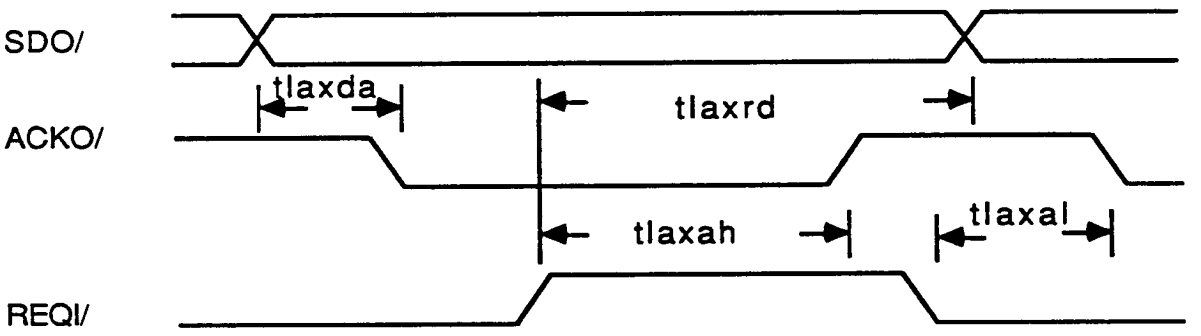
Symbol	Description	Min	Max	Unit
tTarrh	ACKI/ low to REQO/ high		50	ns
tTarrl	ACKI/ high to REQO/ low (FIFO not full)		55	ns



8.2.5 Initiator Asynchronous Transfers

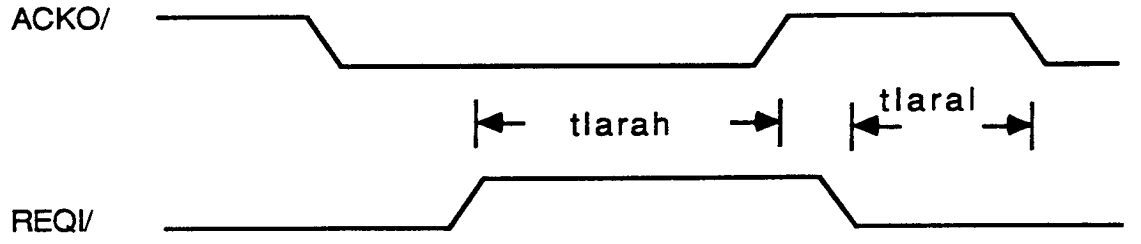
8.2.5.1 Initiator Asynchronous Send

Symbol	Description	Min	Max	Unit
tlaxda	Data to ACKO/ low	65		ns
tlaxah	REQI/ high to ACKO/ high		46	ns
tlaxrd	REQI/ high to data (FIFO bottom full)		80	ns
tlaxal	REQI/ low to ACKO/ low (data already setup)		55	ns



8.2.5.2 Initiator Asynchronous Receive

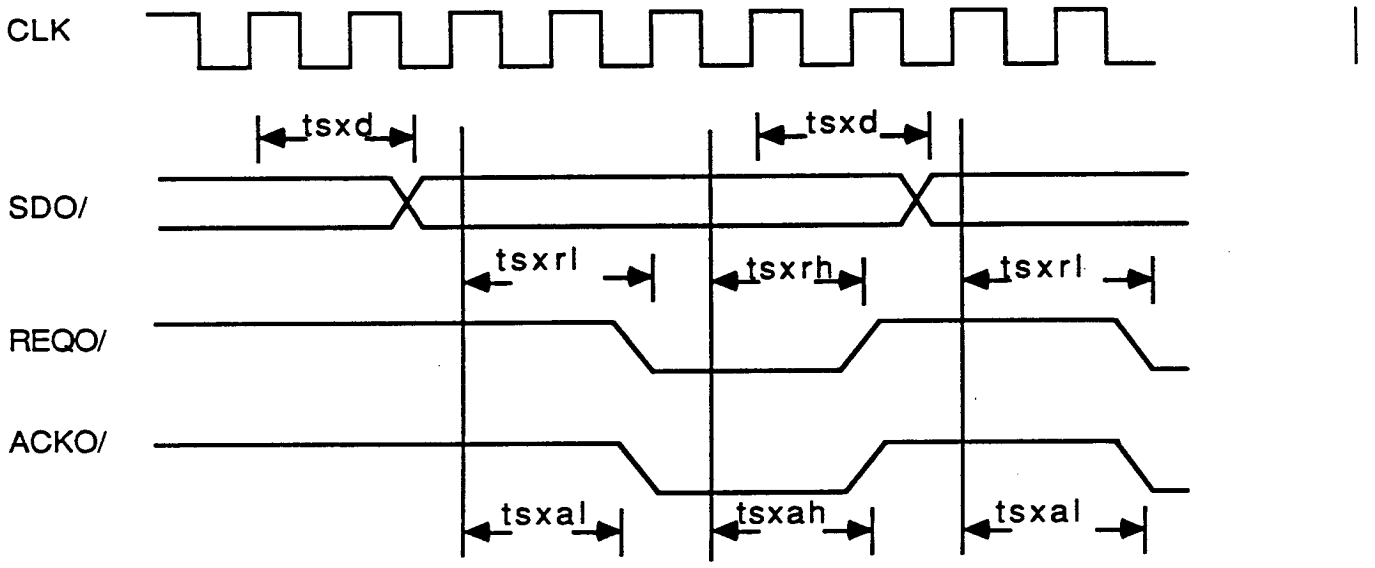
Symbol	Description	Min	Max	Unit
tlarah	REQI/ high to ACKO/ high		50	ns
tlaral	REQI/ low to ACKO/ low (FIFO not full)		68	ns



8.2.6 Synchronous Transfers

8.2.6.1 Target and Initiator Synchronous Transmit

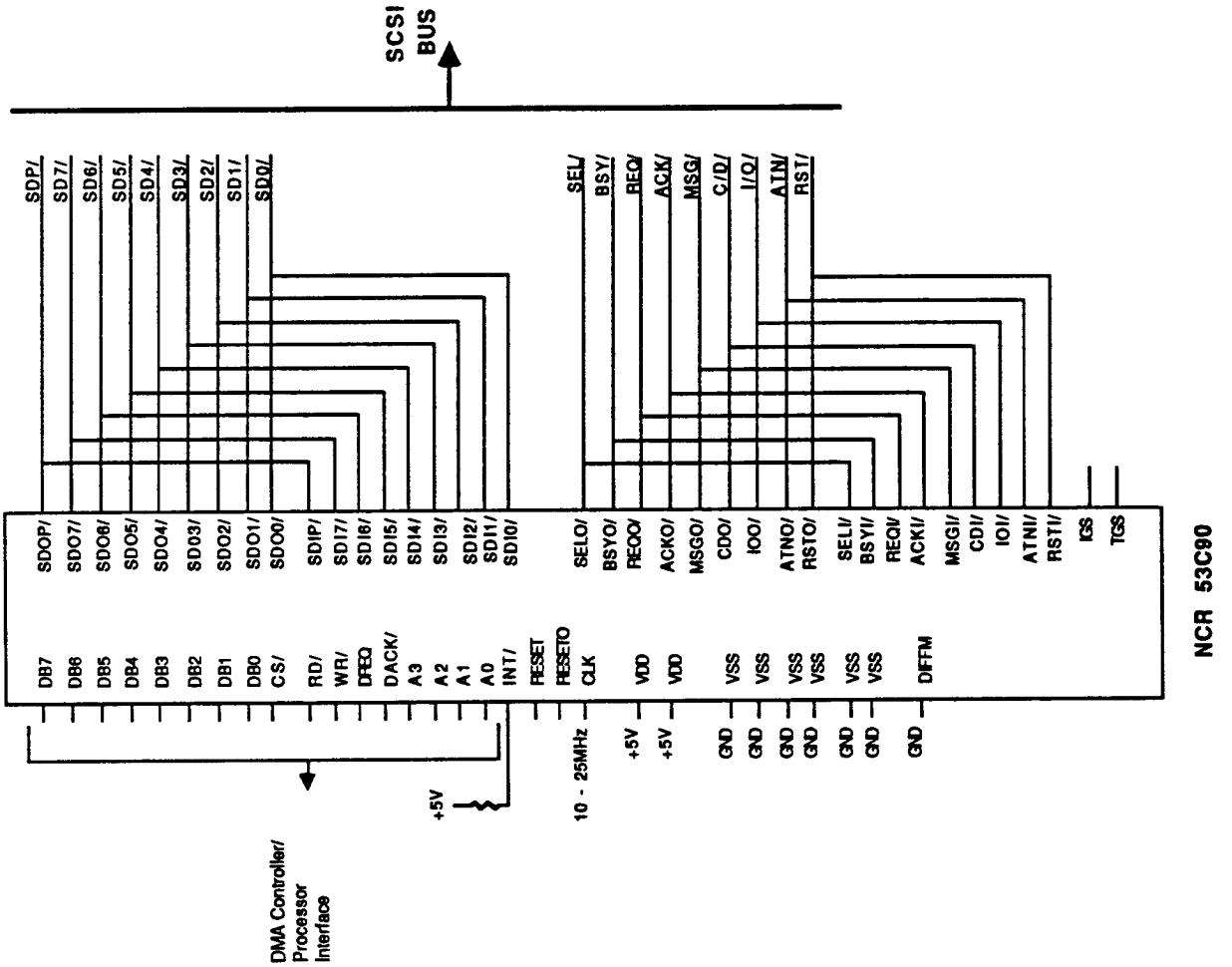
Symbol	Description	Min	Max	Unit
tsxd	Data from CLK high	20	84	ns
tsxrl	REQO/ low from CLK high	15	64	ns
tsxrh	REQO/ high from CLK low	17	69	ns
tsxal	ACKO/ low from CLK high	15	64	ns
tsxah	ACKO/ high from CLK low	17	70	ns



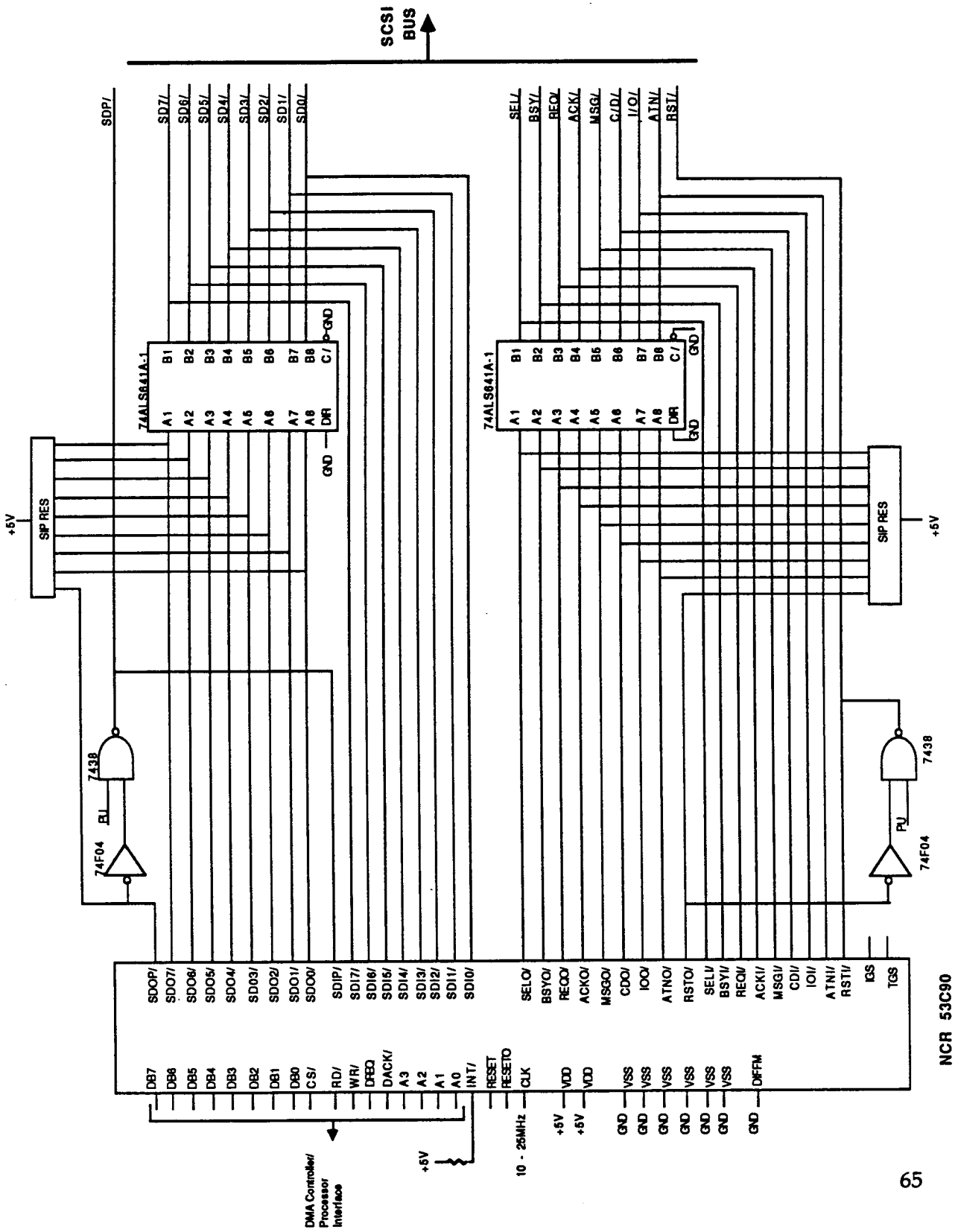
9. APPLICATIONS

9.1 Single-ended Mode

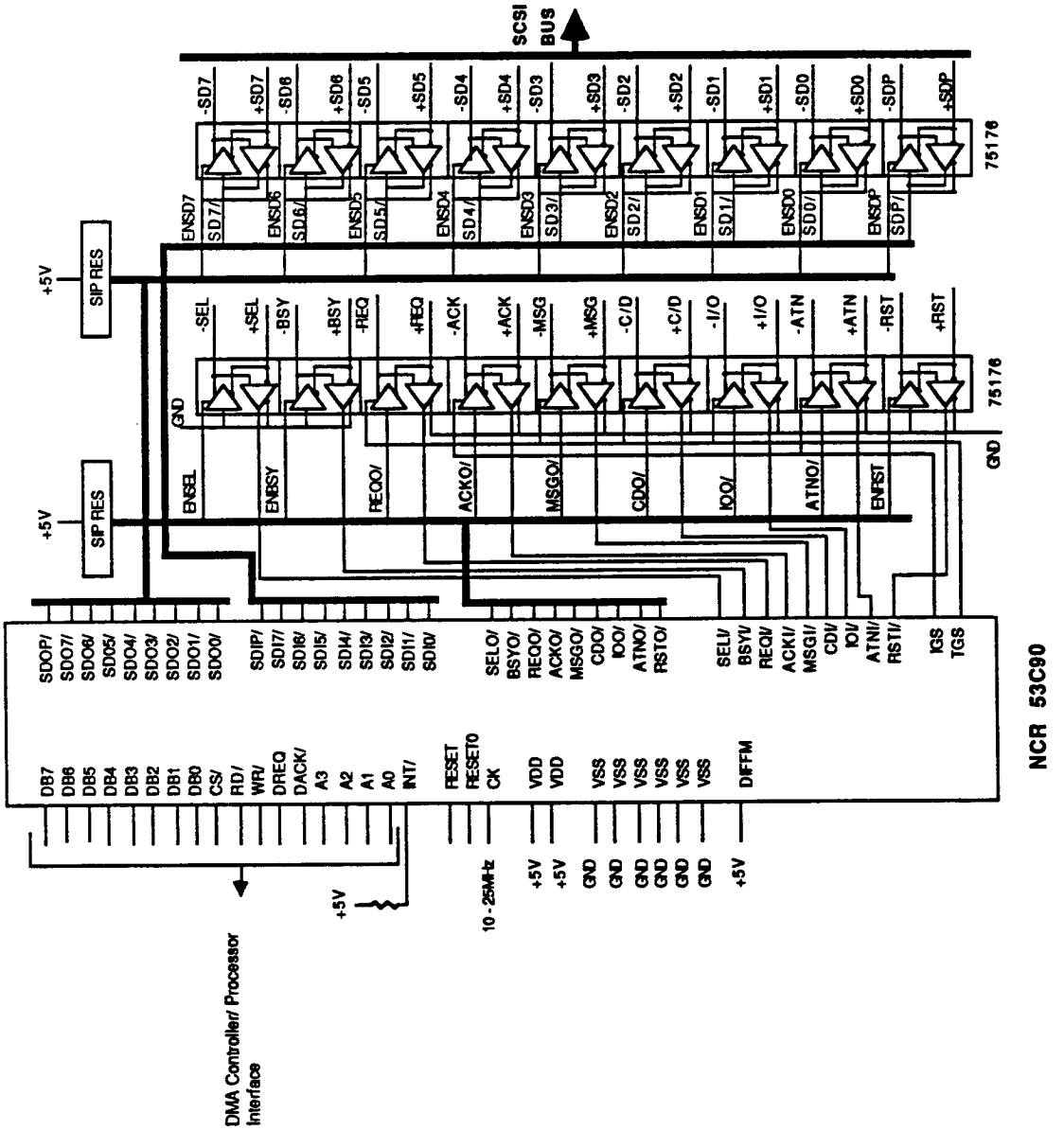
9.1.1 Single-ended Mode without External Drivers



9.1.2 Single-ended Mode with External Drivers



9.2 Differential Mode



APPENDICES

Appendix A - Register Summary

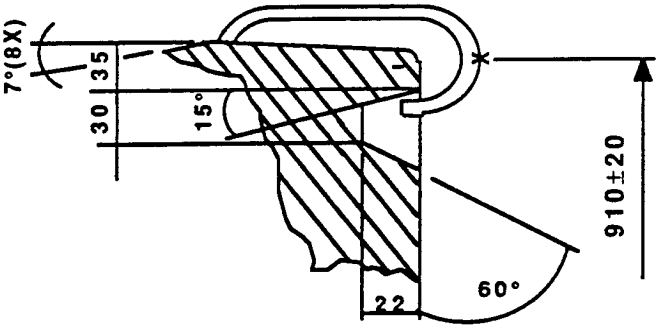
#	ESP Read Registers	#	ESP Write Registers
0	Transfer counter lo(LSB)	0	Transfer count lo (LSB)
1	Transfer counter hi (MSB)	1	Transfer count hi (MSB)
2	FIFO	2	FIFO
3	Command	3	Command
4	Status	4	S/R bus ID
5	Interrupt	5	S/R timeout
6	Sequence step	6	Sync period
7	FIFO flags	7	Sync offset
8	Configuration	8	Configuration
9	NCR Reserved	9	Clock factor
A	Test	A	Test

Command Register (RW3) (Bit 7 Set = DMA Mode)

Misc Cmds	Initiator Cmds	Target Cmds
00 80 NOP 01 81 Flush FIFO 02 82 Reset chip 03 83 Reset SCSI	10 90 Transfer info 11 91 Cmd comp seq 12 92 Accept msg 18 98 Transfer pad 1A 9A Set ATN	20 A0 Send msg 21 A1 Send status 22 A2 Send data 23 A3 Disconnect seq 24 A4 Terminate seq 25 A5 Cmd comp seq 27 A7 Disconnect 28 A8 Rcv msg seq 29 A9 Rcv cmd 2A AA Rcv data 2B AB Rcv cmd seq
Disconnected Cmds		
40 C0 Reconnect 41 C1 Sel w/o ATN 42 C2 Sel w/ATN 43 C3 Sel w/ATN/stop 44 C4 Enable S/R 45 C5 Disable S/R		

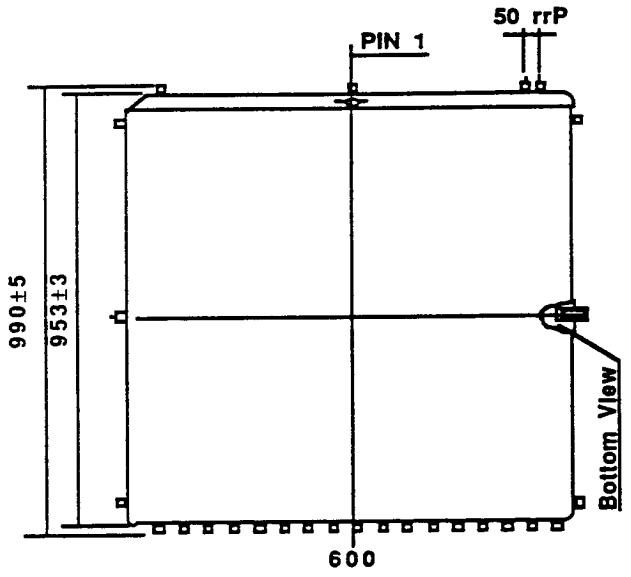
STATUS (RO4)	INT (RO5)	CONFIG (RW8)
0 I/O 1 C/D 2 MSG 3 Xfr complete 4 Xfr count 0 5 Parity error 6 Gross error 7 NCR Reserved	0 Selected 1 Selected w/ATN 2 Reselected 3 Func complete 4 Bus service 5 Disconnect 6 Illegal cmd 7 SCSI reset	0 Bus ID 0 1 Bus ID 1 2 Bus ID 2 3 (0) 4 Parity enable 5 Parity test mode 6 SCSI rst int dis 7 Slow cable
SEQ STEP (RO6)	**TEST (WOA)**	
0 Seq step 0 1 Seq step 1 2 Seq step 2	0 Target Mode 1 Initiator Mode 2 Tri-state Mode	

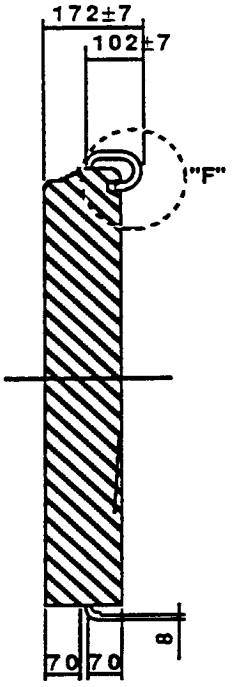
Appendix B - 68 Pin PLCC Mechanical Drawing

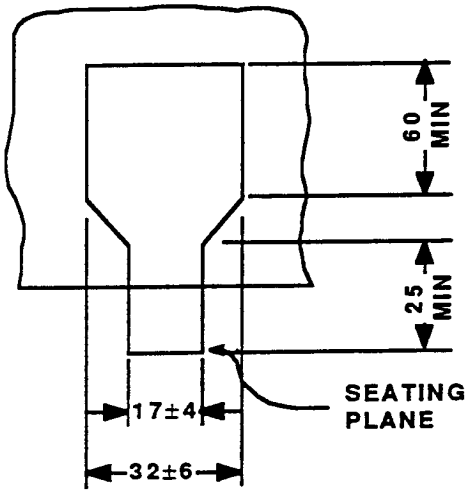


DETAIL OF "F"

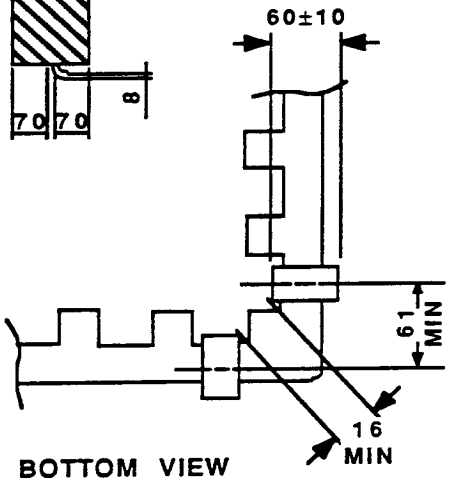
X: SURFACE MOUNT POINT







SIDE VIEW



BOTTOM VIEW